PY32F031 Datasheet

32-bit ARM® Cortex®-M0+ Microcontroller

Puya Semiconductor (Shanghai) Co., Ltd.

Features

- Core
  - — ARM® 32-bit Cortex®-M0+
  - — Frequency up to 72 MHz
- Memories
  - — Up to 64 KB Flash memory
  - — Up to 8 SRAM
  - — 128 Bytes User OTP Data
- Clock management
  - — 4/8/16/22.12/24 MHz High-speed internal RC oscillator (HSI)
  - — 32.768 kHz Low-speed internal RC oscillator(LSI)
  - — 4 - 32 MHz High-speed external crystal oscillator (HSE)
  - — 32.768 kHz Low-speed external crystal oscillator (LSE)
  - — PLL(x2,x3)
- Power management and reset
  - — Operating voltage: 1.7 - 5.5 V
  - — Low-power modes: Sleep, Stop
  - — Power-on/power-down reset (POR/PDR)
  - — Brown-out reset (BOR)
  - — Programmable voltage detector (PVD)
- General-purpose input and output (I/O)
  - — Up to 44 I/Os, all available as external interrupts
- 3-channel DMA controller
- 1 x 12-bit ADC
  - — Up to 10 external and 5 internal channels
  - — Input voltage conversion range: 0 - V_{CC}
  - — Internal reference voltage: 1.024/1.5/2.048/2.5 V
- 4*18/8*14 LCD
- Timers
  - — 1 x 16-bit advanced-control timer (TIM1)
  - — 3 x 16-bit general-purpose timer (TIM14/TIM16/TIM17)
  - — 1 x 32-bit general-purpose timer (TIM2)
  - — 1 x low power timer (LPTIM), supporting wake-up from Stop mode
  - — 1 x independent watchdog timer (IWDG)
  - — 1 x window watchdog timer (WWDG)
  - — 1 x SysTick timer
  - — 1 x IRTIM
- RTC
- Communication interfaces
  - — 2 x serial peripheral interface(SPI), 1 with I^2S interface multiplexed
  - — 3 x universal synchronous/asynchronous receiver/transmitters (USARTs), supporting automatic baud rate detection, 1 with LIN capability.
  - — 1 x I^2C interface, supporting Standard mode(100 kHz), Fast mode (400 kHz), Fast mode plus (1 MHz); with 7-bit addressing mode
- Hardware CRC-32 module
- 2 x comparators
- 2 x operational amplifier
- 32-bit Hardware divider (DIV)
- CORDIC for trigonometric functions acceleration (square root, sine/cosine and arctangent)
- Unique UID
- Serial wire debug (SWD)
- Operating temperature: -40 - 85°C, -40 - 105°C
- Packages: LQFP48, QFN48(6*6), QFN48(5*5), QFN40, LQFP32, QFN32(5*5), QFN32(4*4),

TSSOP20, DFN8 (2*2*0.45)

Content

1. Introduction

The PY32F031 microcontrollers feature the high-performance ARM® 32-bit Cortex®-M0+ core operating at up to 72 MHz frequency, embedded memories with up to 64 KB Flash and 8 KB SRAM, available in multiple package options. The PY32F031 integrates I^2C, SPI, and USART and other communication peripherals, one 12-bit ADC, four 16-bit timers, one 32-bit timers, two comparators, two operational amplifiers, and one LCD driver.

The PY32F031 operates in the -40 - 85°C or -40 - 105 °C temperature ranges from a 1.7 to 5.5 V power supply, and provides Sleep and Stop low power operating modes, which can meet different low-power applications.

These features make the PY32F031 microcontrollers suitable for a wide range of applications such as controllers, portable devices, PC peripherals, gaming and GPS platforms, as well as industrial applications.

Table 1-1PY32F031x6 series product features and peripheral counts

Peripherals		PY32F031C18T6	PY32F031C18U6	PY32F031C28U6	PY32F031H18U6	PY32F031K18T6	PY32F031K18U6	PY32F031F18P6	PY32F031L18D6
Flash (KB)		64	64	64	64	64	64	64	64
SRAM (KB)		8	8	8	8	8	8	8	8
Timers	Advanced control	1 *16-bit							
	General purpose	3*16-bit, 1*32-bit							
	Low power timer	1							
	SysTick	1							
	Watchdog	2							
Comm. interfaces	SPI (I^2S)	2(1)							1(1)
	I^2C	2							1
	USART (LIN)	3(1)							1(1)
DMA		3 ch							
RTC		Yes							
GPIOs		44	44	44	38	30	30	18	7
ADC (external + internal)		10+5	10+5	10+5	10+5	10+5	10+5	9+5	3+5
Comparators		2							1
OPA		2							-
LCD		4*18 / 8*14						-	-
HDIV		Yes							
CORDIC		Yes							
Max. CPU frequency		72 MHz							
Operating voltage		1.7 - 5.5 V							
Operating temperature		-40 - 85 ℃							
Packages		LQFP48	QFN48(6*6)	QFN48(5*5)	QFN40	LQFP32	QFN32(5*5)	TSSOP20	DFN8(2*2)

Table 1-2PY32F031x7 series product features and peripheral counts

Peripherals		PY32F031C18T7	PY32F031K28U7
Flash (KB)		64	64
SRAM (KB)		8	8
Timers	Advanced-control timer	1 *16-bit	
	General-purpose timers	3*16-bit, 1*32-bit	
	Low power timer	1	
	SysTick	1	
	Watchdog	2	
Comm. interfaces	SPI (I^2S)	2(1)	
	I^2C	2	
	USART (LIN)	3(1)	
DMA		3 ch	
RTC		Yes	
GPIOs		44	30
ADC (external + internal)		10+5	
Comparators		2	
Operational amplifier		2	
LCD		4*18 / 8*14	
HDIV		Yes	
CORDIC		Yes	
Max. CPU frequency		72 MHz	
Operating voltage		1.7 - 5.5 V	
Operating temperature		-40 - 105 ℃	
Packages		LQFP48	QFN32(4*4)

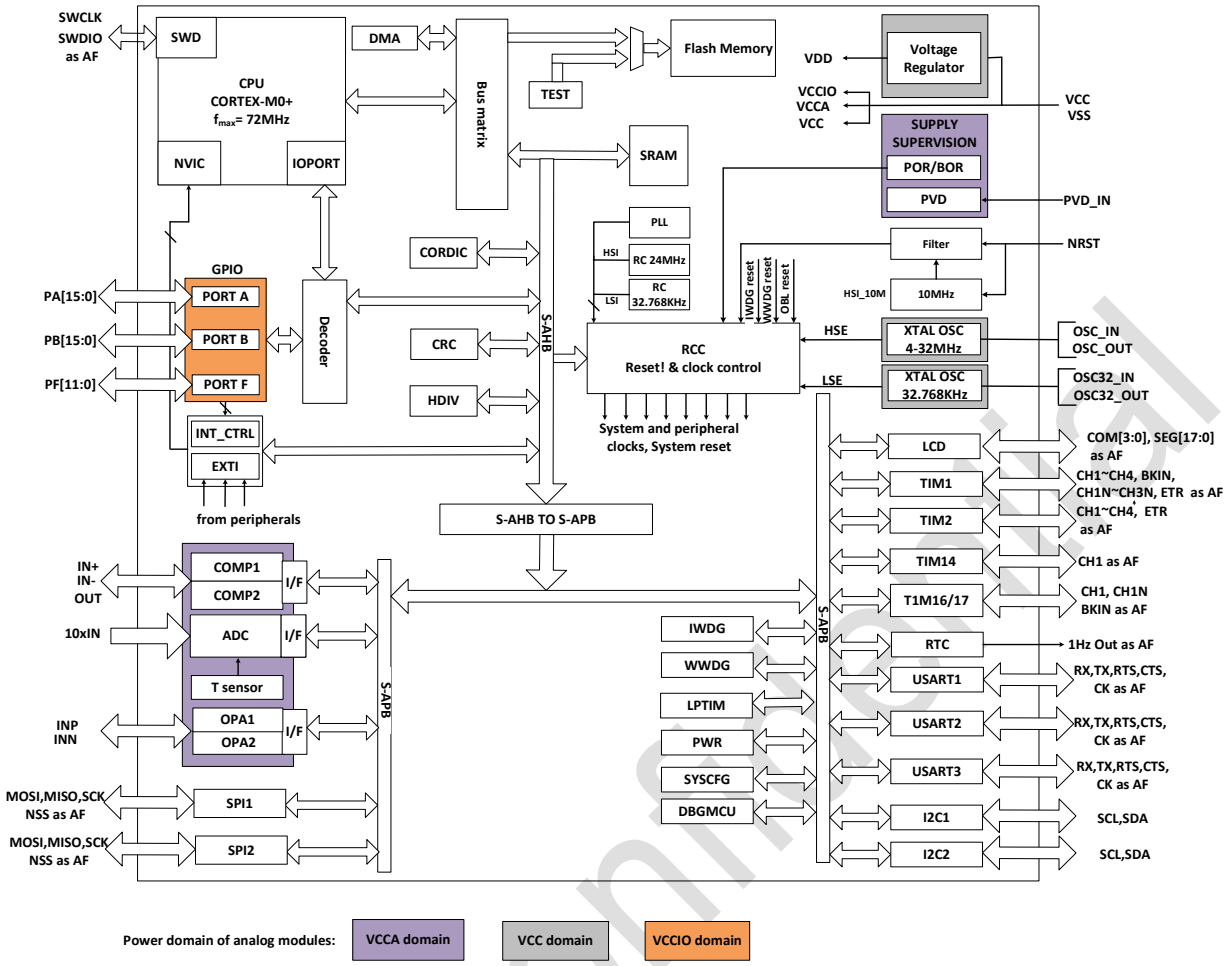


Figure1-1 System block diagram

2. Functional overview

2.1. Arm®-Cortex®-M0+ core

The Arm® Cortex® -M0+ is an Arm 32-bit Cortex processor designed for embedded applications. It provides developers with significant benefits, including:

- Simple architecture for easy learning and programming
- Ultra-low power consumption for energy-efficient operation
- Reduced code density

The Arm® Cortex-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. It delivers high performance through a streamlined instruction set and hardware enhancements like a single-cycle multiplier. Outperforms 8/16-bit MCUs in code efficiency.

The Cortex-M0+ is tightly coupled with a Nested Vectored Interrupt Controller (NVIC).

2.2. Memories

Embedded SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits).

The Flash memory is composed of two distinct physical areas:

- The Main flash area consists of application and user data
- 4 KB of Information area:
  - Option bytes
  - UID bytes
  - System memory
  - User OTP Data

The protection of Main flash area includes the following mechanisms:

- Read protection (RDP) blocks external access
- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 4 KB.
- Option byte write protection is a special design for unlock.

2.3. Boot modes

At startup, the BOOT0 pin and the boot configuration bit nBOOT1 (stored in option bytes) are used to select one of the three boot options in the following table:

Table 2-1 Boot configuration

Boot mode configuration		Mode
nBOOT1 bit	BOOT0 pin	
X	0	Boot from Main flash
1	1	Boot from System memory
0	1	Boot from SRAM

The Boot loader is located in the System memory and is used to reprogram the Flash memory by using USART.

2.4. Clock management

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. After the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- A 4/8/16/22.12/24 MHz configurable internal high precision HSI clock
- A 32.768 kHz configurable LSI clock
- A 4 - 32 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. a CPU NMI interrupt is generated at the same time.
- A 32.768 kHz LSE clock
- System PLL with maximum output frequency of 72 MHz. It can be fed with HSE or HSI clocks. If the HSE source is selected, when CSS is enabled and CSS fails, disable PLL and HSE, and the system clock is automatically switched to HSI.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The maximum frequency of the AHB and the APB domains is 72 MHz.

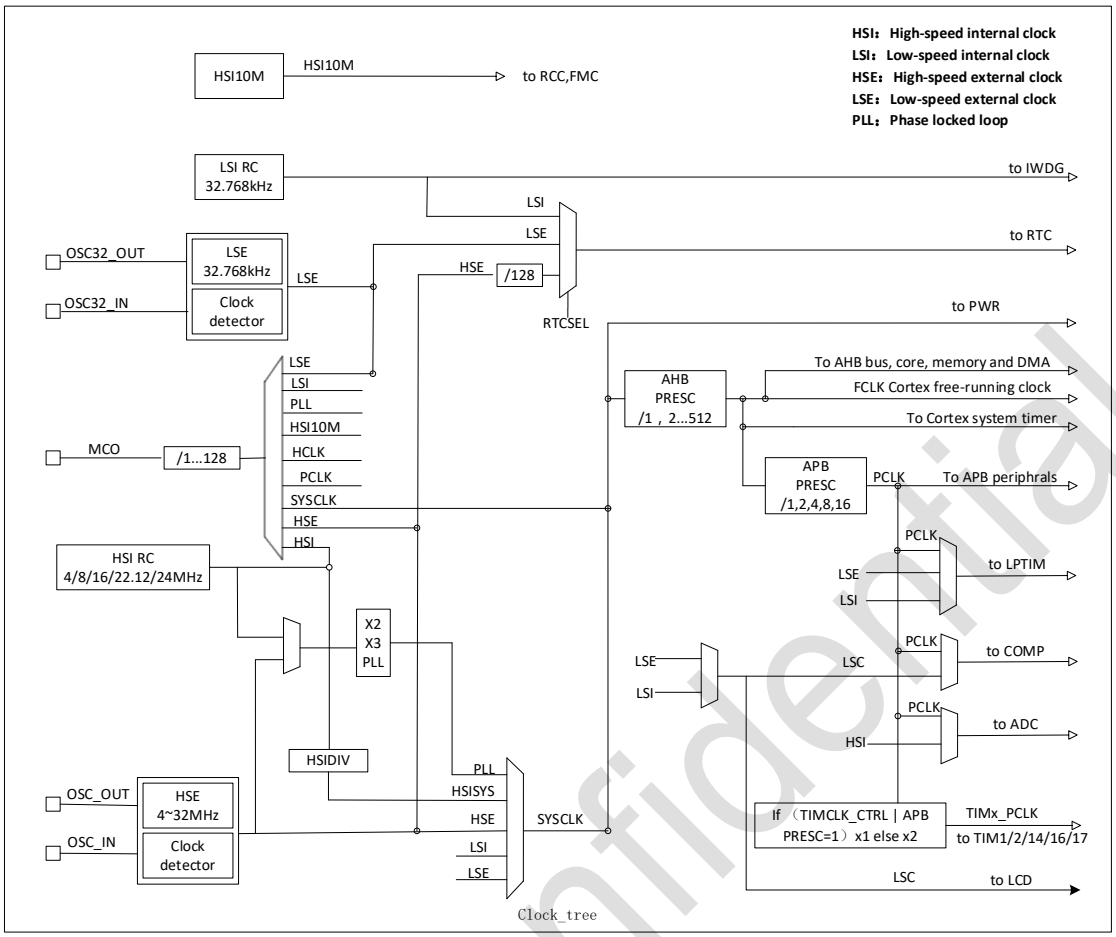


Figure 2-1 System clock structure diagram

2.5. Power management

2.5.1. Power block diagram

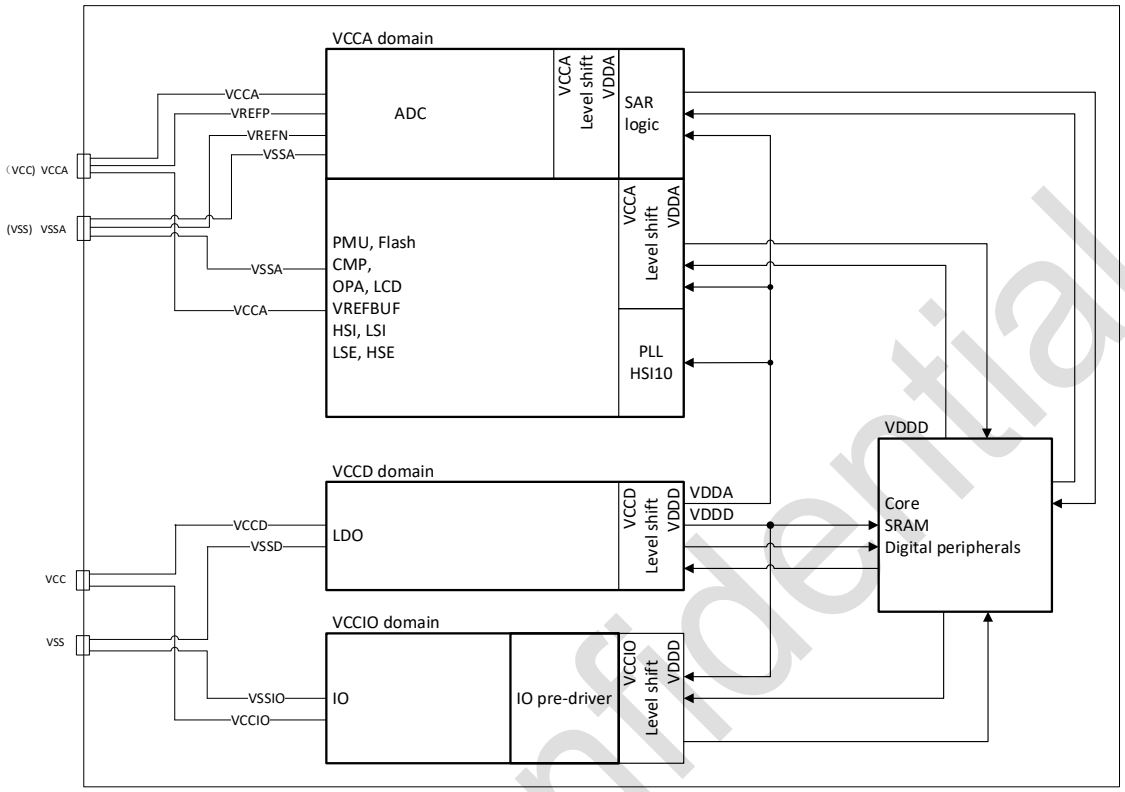


Figure 2-2 Power block diagram

Table 2-2 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	1.7 - 5.5 V	Power supply range: 1.7 - 5.5 V. The power is supplied to the device through the power pins, with the power supply module comprising: Partial analog circuits.
2	V_{CCA}	1.7 - 5.5 V	Powers for most analog modules, sourced from V_{CC}.
3	V_{CCIO}	1.7 - 5.5 V	Power to IO from V_{CC}

2.5.2. Power monitoring

2.5.2.1. Power-on/power-down reset (POR/PDR)

The Power-on reset (POR) and Power-down reset (PDR) module is designed in the chip to provide the module keeps working in all modes. The module keeps working in all modes.

2.5.2.2. Brown-out reset (BOR)

In addition to POR/PDR, BOR (Brown-out reset) is also implemented. BOR can only be enabled and disabled through the Option byte.

When the BOR is turned on, the BOR threshold can be selected by the Option byte and both the rising and falling detection points can be individually configured.

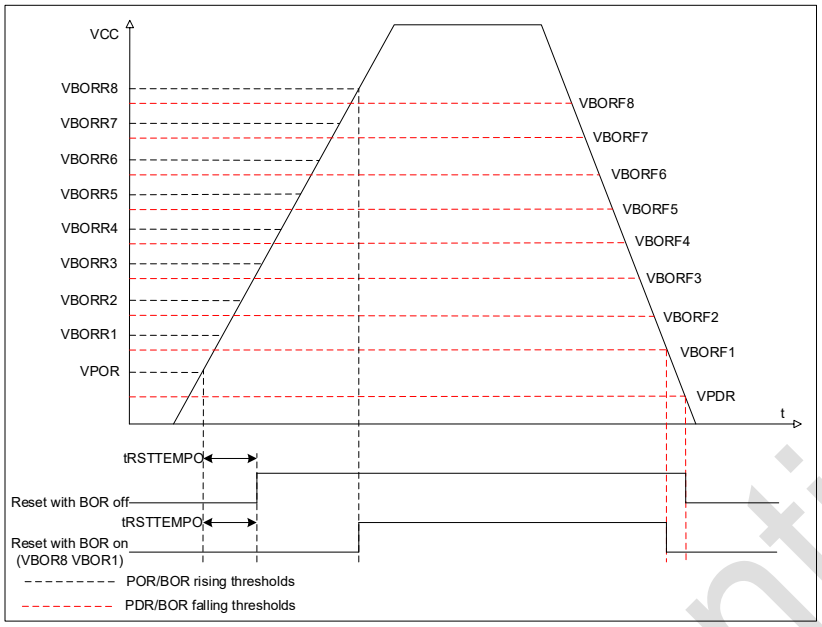


Figure 2-3 POR/PDR/BOR threshold

2.5.2.3. Programmable voltage detector (PVD)

Programmable voltage detector, PVD module can monitor the V_{CC} power supply (or monitor the voltage on the PB7 pin), with the detection point configurable via registers. The device remains in reset mode when the monitored supply voltage V_{CC} is below a specified threshold.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when V_{CC} rises above the detection point of PVD, or V_{CC} falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

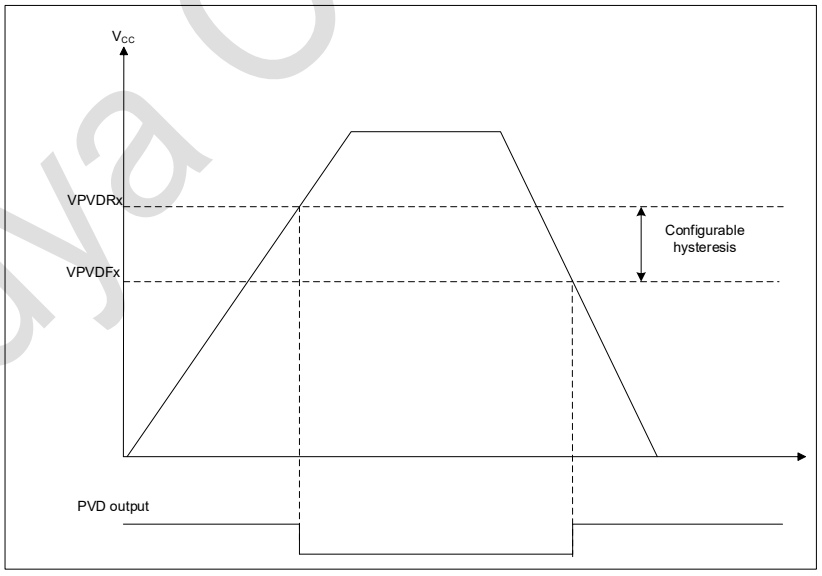


Figure 2-4 PVD threshold

2.5.3. Voltage regulator

The regulator has two operating modes:

- MR (Main regulator) is used in normal operating mode (Run).
- LPR (Low power regulator) provides an option for even lower power consumption in Stop mode.

2.5.4. Low-power mode

In addition to the normal operating mode, the chip has two low-power modes:

- **Sleep mode:** Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works. It is recommended only to enable the modules that must work, and close the module after the module works.
- **Stop mode:** In this mode, SRAM and register contents are retained. PLL, HSI and HSE are turned off and most module clocks in the V_{DDD} domain are disabled. GPIO, PVD, COMP output, RTC, and LPTIM can wake up the Stop mode.

2.6. Reset

- Two resets are designed in the chip: power reset and system reset.

2.6.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out reset (BOR)

2.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load (OBL) reset

2.7. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating, pull-up or pull-down and analog) or as peripheral alternate function. The I/O configuration can be locked.

2.8. Hardware divider

Hardware divider is a 32-bit signed/unsigned integer hardware divider.

The hardware divider supports the following features:

- Configurable signed/unsigned division calculation

- 32-bit dividend, 32-bit divisor
- Outputs 32-bit quotient and 32-bit remainder
- Divide-by-zero warning flag bit, end-of-division flag bit
- 8 clock cycles to complete a division operation
- Write the divisor register to trigger the start of the division circuit
- Reading the quotient register/remainder register automatically waits for the calculation to complete

2.9. CORDIC digital signal processor

The CORDIC digital signal processor provides hardware acceleration for mathematical functions, commonly used in applications such as motor control, metering, and signal processing. A hardware-accelerated computing module that includes square root operations and trigonometric functions (sine, cosine, arctangent), supporting fixed-point square root and trigonometric operations. Trigonometric functions support 360°/2^16 operation precision.

2.9.1. Hardware Square Root

The radicand is a 32-bit unsigned number, and the square root is a 16-bit unsigned number.

- 16 bus cycles completed
- Configurable signed/unsigned division calculation

2.9.2. Sine/Cosine and arctangent operations

The trigonometric CORDIC module has a bit width of 16 bits, in Q15 fixed-point format.

2.10. DMA

- Direct memory access (DMA) is used to provide a high-speed data transfer between peripherals and memory as well as from memory to memory.
- The DMA controller have 3 channels in total, each one dedicated to manage memory access requests from one or more peripherals. The DMA controller includes an arbiter to handle DMA requests, which manages the priority of each DMA request.
- DMA supports circular buffer management, eliminating the need for user code intervention when the controller reaches the end of the buffer.
- Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
- DMA can be used for major peripherals: SPI, I^2C, USART, LCD, ADC and all TIMx timers (except TIM14 and LPTIM).

2.11. Interrupts and events

The PY32F031 handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.11.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Support 1 NMI
- Support 28 maskable external interrupts
- Support 6 Cortex-M0+ exceptions
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.11.2. Extended interrupt/event controller (EXTI)

- EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from Stop mode.
- The EXTI controller has multiple channels, including up to 44 GPIOs multiplexed using 16 EXTI lines, 1 PVD output, 2 COMP outputs, as well as RTC and LPTIM Wake-up signals. GPIO, PVD and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 15 channel through the select signal.
- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.12. Analog-to-digital converter (ADC)

- The chip has a 12-bit SAR-ADC. The module has a total of up to 15 channels to be measured, including 10 external and 5 internal channels. The internal voltage reference: V_{REFBUF} (1.024V, 1.5 V, 2.048 V, 2.5 V) or the power supply voltage.
- Internal channels include T_S, V_{REFINT}, V_{CC}/3, OPA1_OUT, OPA2_OUT.
- A/D conversion of the various channels can be performed in single, continuous, or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.
- The channel priority conversion sequence can be set when multiple channels are selected.
- The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.
- An efficient low-power mode is implemented to allow very low consumption at low frequency.
- Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers.

2.13. Comparators (COMP)

The device integrates two general-purpose comparators (COMP), which can also be used in combination with Timer. Comparators can be used as :

- Triggered by analog signal to wake-up function from low-power mode
- Analog signal conditioning
- Cycle by cycle current control loop when comparators are connected with PWM output from timer.

2.13.1. COMP main features

- Each comparator has configurable positive or negative input for flexible voltage selection:
  - Multiple I/O pins
  - Power supply V_{CC}
  - Output of the temperature sensor
  - 64-step voltage division supporting internal reference voltage V_{REFBUF} and V_{CC}
  - OPA output as INP input
- Configurable hysteresis function
- Programmable speed and consumption
- The output can be triggered by a connection to the I/O or timer input
  - OCREF_CLR event (cycle by cycle current control)
  - Brakes for fast PWM shutdown
  - Timer IC input

- COMP1 and COMP2 can be combined into window COMP
- Configurable digital filter

2.14. Operational amplifier (OPA)

The OPA1/2 modules can be flexibly configured for simple filter and buffer applications.

2.15. Hardware divider (DIV)

Hardware divider is a 32-bit signed/unsigned integer hardware divider.

DIV features:

- Support 32-bit division
- The data in the register cannot be changed while the current division is not finished
- Configurable signed/unsigned division calculation
- 32-bit dividend, 32-bit divisor
- Outputs 32-bit quotient and 32-bit remainder
- Divide-by-zero warning flag bit, end-of-division flag bit
- 16 clock cycles to complete one division operation
- Write the divisor register to trigger the start of the division circuit
- After writing the divisor, when reading the quotient and remainder registers, you need to wait for the completion flag DIV_END
- When the divisor is 0, the result of quotient and remainder is 0

2.16. Liquid crystal display (LCD) controller

The LCD controller is a digital controller/driver for monochrome passive liquid crystal displays (LCD), with up to 8 common terminals (COM) and 18 segment terminals (SEG) to drive 72 (4 * 18) or 122 (8 * 14) LCD pixels. The exact number of terminals depends on the device pins described in the data manual.

2.17. Timers

The different timers feature as blow:

Table 2-3 Timer characteristics

Timer type	Timer	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Complementary outputs
Advanced-control timer	TIM1	16-bit	Up, down, up/down	1 - 65536	Yes	4	3
General-purpose timers	TIM2	32-bit	Up, down, up/down	1 - 65536	Yes	4	-
	TIM14	16-bit	Up	1 - 65536	-	1	-

Timer type	Timer	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Complementary outputs
	TIM16,TIM17	16-bit	Up	1 - 65536	Yes	1	1

2.17.1. Advanced-control timer

- 16-bit auto-reload counter with up, down, or up/down counting capability
- 16-bit programmable divider, allowing the clock frequency of the counter to be divided by 1 to 65536.
- Up to 4 independent channels
  - Input capture
  - Output compare
  - PWM generation (edge or center-aligned mode)
  - Single pulse mode output
  - Retriggerable single-pulse mode output
- Complementary outputs with programmable dead time
- Synchronization circuit using external signals to control timers and interconnect timers
- Repetition counter to update the timer registers only after a given number of cycles of the counter.
- Output signal of the timer can be set as reset and know state by break input.
- Interrupt/DMA occurs on the following events
  - Update: Counter overflow (up/down), counter initialization (via software or internal/external trigger)
  - Trigger event
  - Input capture
  - Output compare
  - Brake input
- Support for incremental (quadrature) encoders and Hall sensor circuits for positioning
- Trigger input for external clock or cycle-by-cycle current management

2.17.2. General-purpose timers

2.17.2.1. TIM2

- The TIM2 general-purpose timer consists of a 32-bit auto-reload counter driven by a 32-bit programmable prescaler. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.
- TIM2 can work with the TIM1 by the Timer Link.
- TIM2 supports the DMA function.

- This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.
- The counter can be frozen in debug mode.

2.17.2.2. TIM14

- The general-purpose timer TIM14 is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM14 features two single channel for input capture/output compare, PWM or one-pulse mode output.
- The counter can be frozen in debug mode.

2.17.2.3. TIM16/TIM17

- TIM16 and TIM17 consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM16/TIM17 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- TIM16/TIM17 have complementary outputs with dead time.
- TIM16/TIM17 supports DMA function.
- The counter can be frozen in debug mode.

2.17.3. Low power timer

- LPTIM is a 16 -bit upcounter with a 3-bit prescaler and support a single count.
- LPTIM can be configured as a Stop mode wake-up source.
- The counter can be frozen in debug mode.

2.17.4. IWDG

- Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.
- The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.
- IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.
- Controlling of option byte can enable IWDG hardware mode.
- IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.
- The counter can be frozen in debug mode.

2.17.5. WWDG

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

2.17.6. SysTick timer

SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.18. Real-time clock (RTC)

- The RTC is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.
- RTC is a 32-bit programmable counter with a prescaler factor of up to 2^{20} bits.
- RTC counter clock source can be LSE/LSI and the stop wake-up source.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).
- RTC supports clock calibration.
- RTC can be frozen in debug mode.

2.19. Inter-integrated circuit interface (I^2C)

The I^2C (Inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I^2C bus. It provides multimaster capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode plus (Fm+).

For specific needs, DMA can be used to reduce the burden on the CPU.

2.20. Universal synchronous/asynchronous receiver transmitter (USART)

The PY32F031 includes 3 USARTs, with USART1 supporting LIN.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baud rate detection
- Programmable data length of 8 or 9 bits
- Configurable stop bit (1 or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Receive/transmit bytes by DMA buffer
- Transfer detection flag
  - Receive buffer full
  - Send empty buffer
  - End of transmission flags
- Parity control
  - Transmit parity bit
  - Check the received data byte
- Flagged interrupt sources
  - CTS change
  - Transmit data register empty
  - Transmission complete
  - Receive full data register
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Detection error
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

2.21. Serial peripheral interface (SPI)

The PY32F031 includes 2 SPIs, with SPI1 supporting I²S.

SPIs allow the chip to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- Master mode baud rate prescaling factors (Max $f_{PCLK}/2$)
- Slave mode frequency (Max $f_{PCLK}/4$)
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Hardware CRC feature for reliable communication
  - In transmit mode, the CRC value can be transmitted as last byte
  - In full-duplex mode, the last received byte is automatically checked for CRC.
- Motorola mode
- Can trigger interrupt-causing Master mode faults, overrun errors and CRC errors
- Two embedded Rx and Tx FIFOs with DMA capability, depth of four, and width of 16 bits (8 bits when data frame is set to 8-bit)

2.22. SWD

An ARM SWD interface allows serial debugging tools to be connected to the PY32F031.

3. Pinouts and pin descriptions

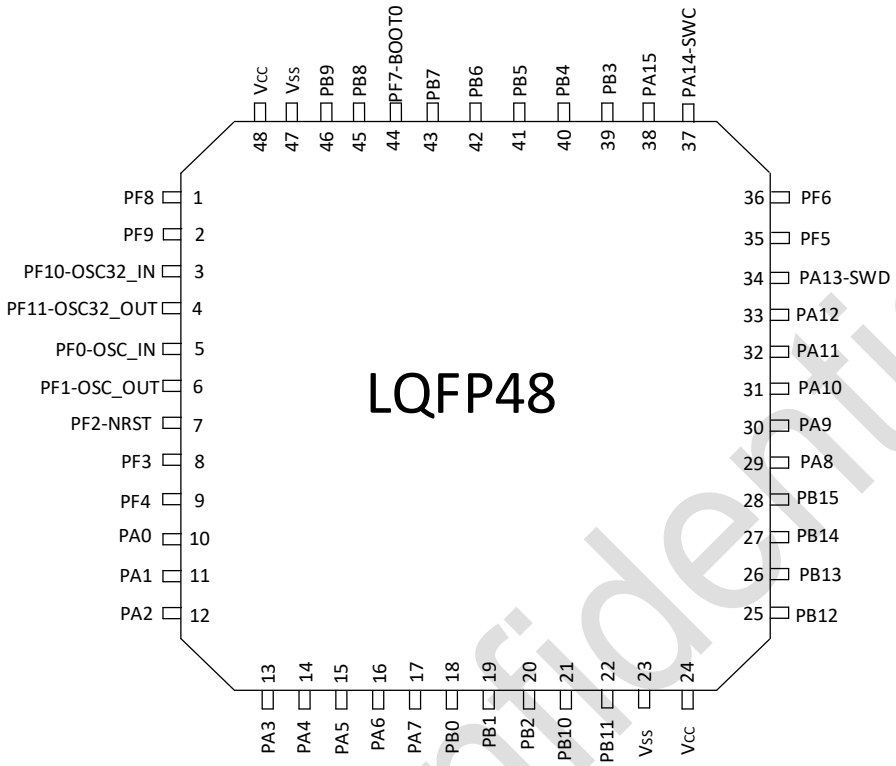


Figure 3-1 LQFP48 Pinout1 PY32F031C1xTx (Top view)

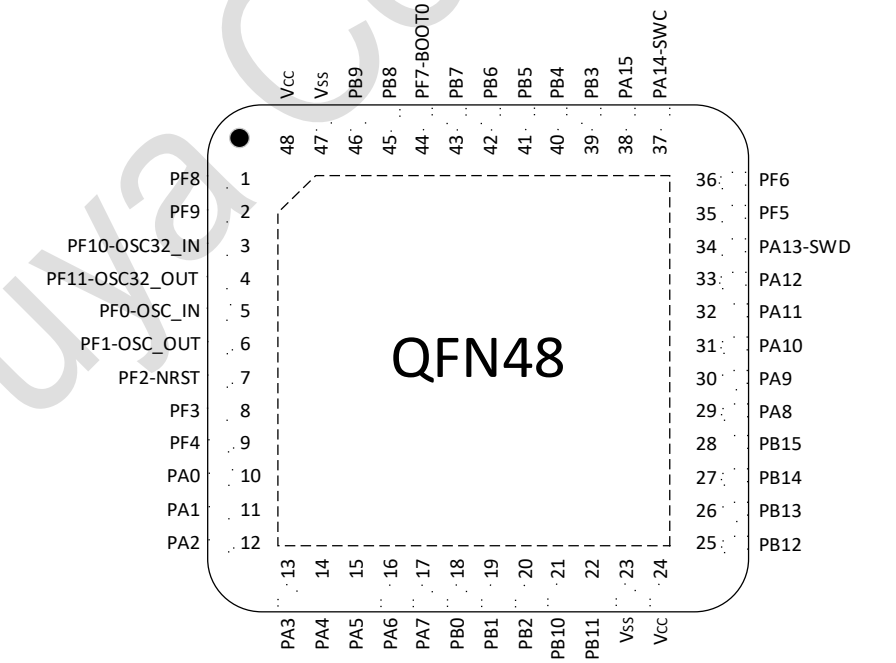


Figure 3-2 QFN48(6*6) Pinout1 PY32F031C1xU6 (Top view)

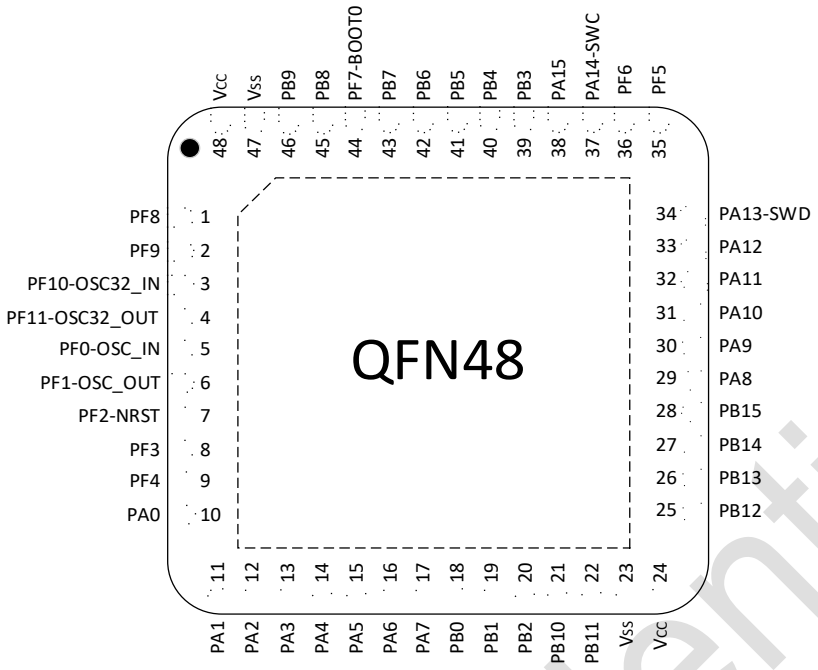


Figure 3-3 QFN48(5*5) Pinout2 PY32F031C2xU6 (Top view)

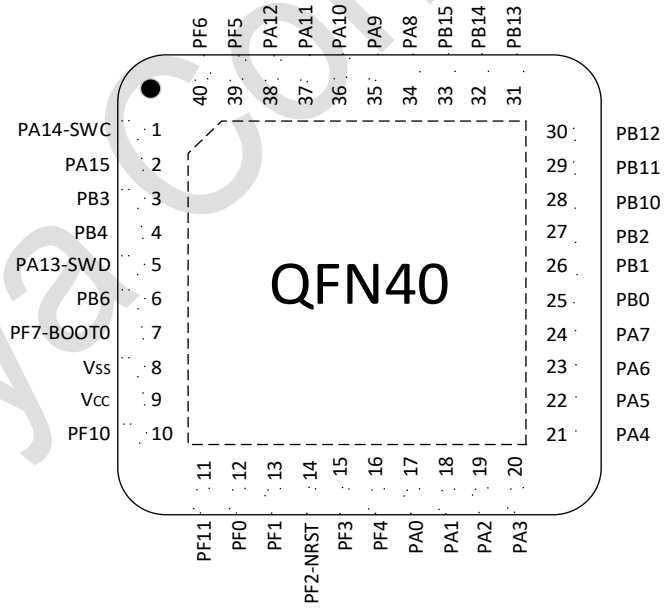


Figure 3-4 QFN40 Pinout1 PY32F031H1xU6 (Top view)

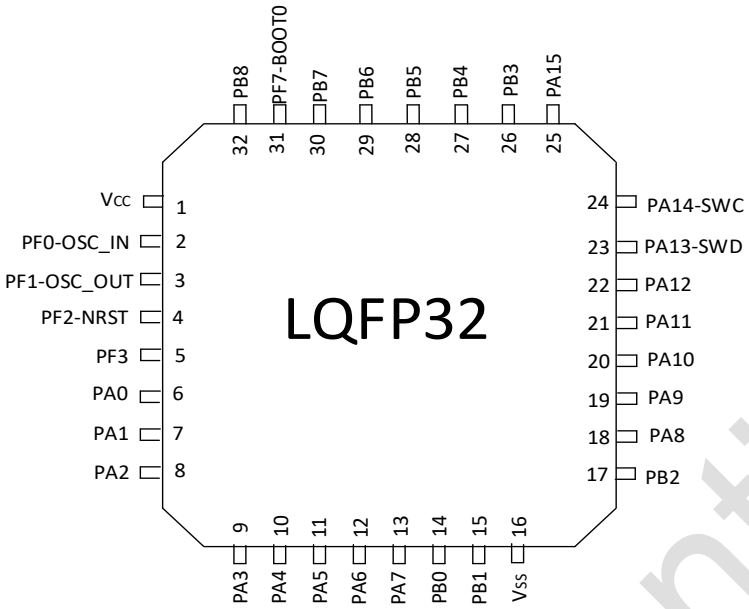


Figure 3-5 LQFP32 Pinout1 PY32F031K1xT6 (Top view)

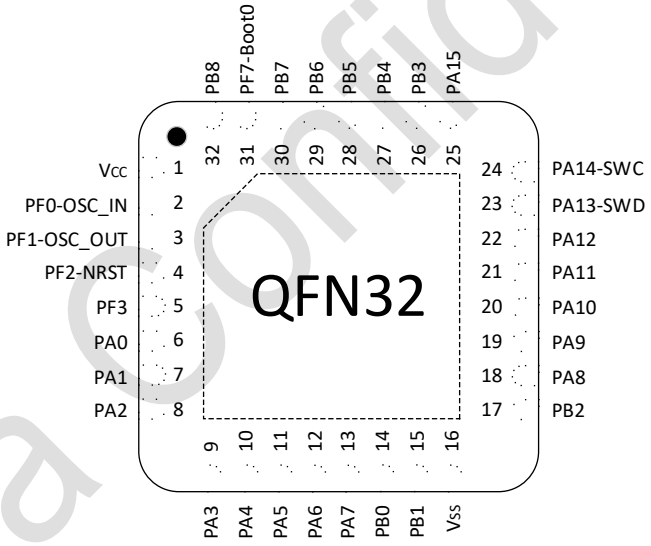


Figure 3-6 QFN32(5*5) Pinout1 PY32F031K1xU6 (Top view)

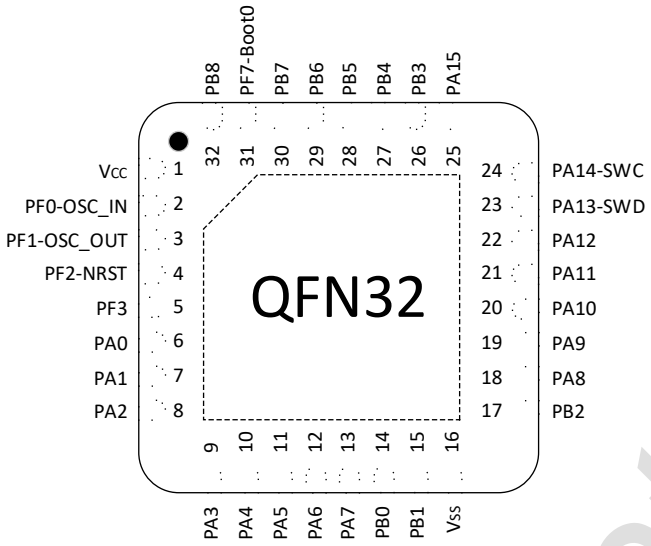


Figure 3-7 QFN32(4*4) Pinout2 PY32F031K2xU7 (Top view)

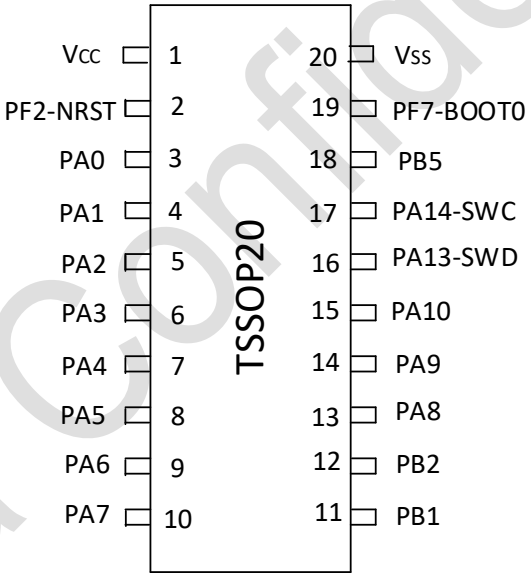


Figure 3-8 TSSOP20 Pinout1 PY32F031F1xP6 (Top view)

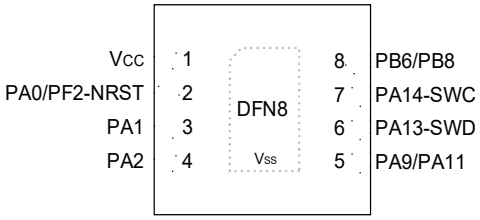


Figure 3-9DFN8(2*2) Pinout1 PY32F031L1xD6 (Top view)

Table 3-1 Legend/abbreviations used in the pinout table

Timer type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I/O	Input / output pin
		NC	No internal connection
I/O structure		COM	Standard 5 V I/O, with Analog switch function supplied by V_{CCA}
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		_L	LED COM port supports analog input/output functions
		_F	I^2C Fm+ with analog input function
		_PU	Internal pull-up resistor
Note		-	Unless otherwise specified, all ports are used as analog inputs between and after reset
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers

Table 3-2 Pin definitions

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
-	-	-	-	1	PF8	I/O	COM		TIM1_CH1 SPI2_MOSI USART2_RX MCO	-
-	-	-	-	2	PF9	I/O	COM		TIM2_CH1 TIM1_CH1N SPI2_SCK USART2_TX	LCD_SEG11
-	-	-	10	3	PF10-OSC32_IN	I/O	COM		-	OSC32_IN
-	-	-	11	4	PF11-OSC32_OUT	I/O	COM		-	OSC32_OUT
-	-	2	12	5	PF0-OSC_IN	I/O	COM_F		SPI2_SCK USART2_RX TIM14_CH1 USART1_RX USART2_TX I2C1_SDA I2C2_SDA	OSC_IN LCD_SEG10
-	-	3	13	6	PF1-OSC_OUT	I/O	COM_F		SPI2_MISO USART2_TX USART1_TX USART2_RX I2C1_SCL I2C2_SCL	OSC_OUT LCD_SEG9

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									SP1_NSS/I2S1_WS	
									TIM14_CH	
2	2	4	14	7	PF2-NRST	I/O	COM	(1)	MCO	NRST
									SPI2_MOSI	
									USART2_RX	
									TIM2_CH2	
									TIM1_CH2	
									TIM1_CH1N	
-	-	5	15	8	PF3	I/O	COM		USART1_TX	COMP2_INP5 LCD_SEG8
									USART2_TX	
									SPI2_MISO	
									SPI1_NSS/I2S1_WS	
									TIM2_CH3	
									RTC_OUT	
-	-	-	16	9	PF4	I/O	COM		-	-
2	3	6	17	10	PA0	I/O	COM_L		SPI2_SCK	ADC_IN0 COMP1_INM1 LCD_SEG7
									USART1_CTS	
									USART2_CTS	
									COMP1_OUT	
									TIM1_CH3	
									TIM1_CH1N	
									IR_OUT	
									USART3_CTS	
									USART2_TX	

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									SPI1_MISO/I2S1_MCK	
3	4	7	18	11	PA1	I/O	COM		SPI1_SCK/I2S1_CK	ADC_IN1 COMP1_INP2 LCD_SEG6
									USART1_RTS	
									USART2_RTS	
									EVENTOUT	
									USART3_RX	
									SPI1_MOSI/I2S1_SD	
									USART2_RX	
									USART3_RTS	
									TIM1_CH4	
									TIM1_CH2N	
									MCO	
4	5	8	19	12	PA2	I/O	COM_F		SPI1_MOSI/I2S1_SD	ADC_IN2 COMP2_INM2 LCD_SEG5
									USART1_TX	
									USART2_TX	
									COMP2_OUT	
									SPI1_SCK/I2S1_CK	
									TIM2_CH1	
									I2C1_SDA	
									I2C2_SDA	
-	6	9	20	13	PA3	I/O	COM_F		SPI2_MISO	ADC_IN3 COMP2_INP4 LCD_SEG4
									USART1_RX	
									USART2_RX	
									EVENTOUT	

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									SPI1_MOSI/I2S1_SD	
									TIM1_CH1	
									I2C1_SCL	
									I2C2_SCL	
-	7	10	21	14	PA4	I/O	COM		SPI1_NSS/I2S1_WS	ADC_IN4 COMP2_INP3 LCD_SEG3
									USART1_CK	
									SPI2_MOSI	
									TIM14_CH1	
									USART2_CK	
									ENENTOUT	
									TIM2_CH3	
									USART2_TX	
									USART3_TX	
									RTC_OUT	
-	8	11	22	15	PA5	I/O	COM		SPI1_SCK/I2S1_CK	ADC_IN5 COMP2_INP2 LCD_SEG2
									EVENTOUT	
									TIM2_CH2	
									USART2_RX	
									MCO	
-	9	12	23	16	PA6	I/O	COM		SPI1_MISO/I2S1_MCK	ADC_IN6
									TIM2_CH1	
									TIM1_BKIN	
									TIM16_CH1	
									COMP1_OUT	

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									USART1_CK	
									RTC_OUT	
-	-	13	24	17	PA7	I/O	COM_F		SPI1_MOSI/I2S1_SD	ADC_IN7
									TIM2_CH2	
									TIM1_CH1N	
									TIM14_CH1	
									TIM17_CH1	
									EVENTOUT	
									COMP2_OUT	
									USART1_TX	
									USART2_TX	
									I2C1_SDA	
									I2C2_SDA	
									SPI1_MISO/I2S1_MCK	
-	10	14	25	18	PB0	I/O	COM		SPI1_NSS/I2S1_WS	ADC_IN8
									TIM2_CH3	
									TIM1_CH2N	
									EVENTOUT	
									COMP1_OUT	
									USART3_CK	
-	11	15	26	19	PB1	I/O	COM		TIM14_CH1	ADC_IN9 COMP1_INM0
									TIM2_CH4	
									TIM1_CH3N	
									EVENTOUT	

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									USART3_RTS	
-	12	17	27	20	PB2	I/O	COM_L		USART1_RX	COMP1_INP1 LCD_SEG1
									USART2_RX	
									TIM1_CH2	
									USART3_RX	
									SPI2_SCK	
-	-	-	28	21	PB10	I/O	COM_F		SPI2_SCK	-
									TIM2_CH3	
									USART3_TX	
									I2C2_SCL	
									I2C1_SCL	
-	-	-	29	22	PB11	I/O	COM_F		TIM2_CH4	-
									USART3_RX	
									EVENTOUT	
									I2C1_SDA	
									I2C2_SDA	
-	-	16	-	23	V_{SS}	G	-		Ground	
-	-	-	-	24	V_{CC}	S	-		Digital power supply	
-	-	-	30	25	PB12	I/O	COM		SPI2_NSS/I2S1_WS	-
									SPI2_NSS	
									TIM1_BKIN	
									EVENTOUT	
									USART3_RTS	
									TIM1_BKIN	

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
-	-	-	31	26	PB13	I/O	COM		SPI2_SCK TIM1_CH1N SPI1_SCK/I2S1_CK USART3_CTS	-
-	-	-	32	27	PB14	I/O	COM		SPI2_MISO TIM1_CH2N SPI1_MISO/I2S1_MCK USART3_RTS	-
-	-	-	33	28	PB15	I/O	COM		SPI2_MOSI TIM1_CH3N SPI1_MOSI/I2S1_SD	-
-	13	18	34	29	PA8	I/O	COM_F		SPI2_NSS USART1_CK TIM1_CH1 USART2_CK MCO EVENTOUT USART1_RX USART2_RX SPI1_MOSI/I2S1_SD I2C1_SCL I2C2_SCL	OPA1_OUT LCD_SEG0
5	14	19	35	30	PA9	I/O	COM_F		SPI2_MISO USART1_TX	OPA1_INP LCD_COM0

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									TIM1_CH2	
									USART2_TX	
									MCO	
									I2C1_SCL	
									EVENTOUT	
									I2C1_SDA	
									I2C2_SDA	
									TIM1_BKIN	
									SPI1_SCK/I2S1_CK	
									USART1_RX	
-	15	20	36	31	PA10	I/O	COM_F		SPI2_MOSI	OPA1_INN LCD_COM1
									USART1_RX	
									TIM1_CH3	
									TIM17_BKIN	
									USART2_RX	
									I2C1_SDA	
									EVENTOUT	
									I2C1_SCL	
									I2C2_SCL	
									SPI1_NSS/I2S1_WS	
									USART1_TX	
5	-	21	37	32	PA11	I/O	COM_F		SPI1_MISO/I2S1_MCK	LCD_COM2
									USART1_CTS	
									TIM1_CH4	

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									EVENTOUT	
									USART2_CTS	
									I2C1_SCL	
									COMP1_OUT	
									I2C2_SCL	
-	-	22	38	33	PA12	I/O	COM_F		SPI1_MOSI/I2S1_SD	LCD_COM3
									USART1_RTS	
									TIM1_ETR	
									USART2_RTS	
									EVENTOUT	
									I21C_SDA	
									COMP2_OUT	
									I2C2_SDA	
6	16	23	5	34	PA13-SWDIO	I/O	COM	(2)	SWDIO	-
									IR_OUT	
									EVENTOUT	
									SPI1_MISO/I2S1_MCk	
									TIM1_CH2	
									USART1_RX	
									MCO	
-	-	-	39	35	PF5	I/O	COM_PU		IR_OUT	-
									EVENTOUT	
									USART1_RX	
									SPI1_MISO/I2S1_MCK	

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									I2C2_SCL	
									I2C2_SDA	
									TIM1_CH2	
-	-	-	40	36	PF6	I/O	COM_PU		USART1_TX	-
									TIM1_CH2N	
									USART2_TX	
									EVENTOUT	
									I2C2_SDA	
									I2C2_SCL	
7	17	24	1	37	PA14-SWCLK	I/O	COM	(2)	SWCLK	-
									USART1_TX	
									USART2_TX	
									EVENTOUT	
									MCO	
									SPI1_SCK/I2S1_CK	
									USART3_TX	
-	-	25	2	38	PA15	I/O	COM_L		SPI1_NSS/I2S1_WS	OPA2_INN LCD_COM4/SEG17
									USART1_RX	
									USART2_RX	
									EVENTOUT	
									USART3_RX	
-	-	26	3	39	PB3	I/O	COM_L		SPI1_SCK/I2S1_CK	OPA2_INP COMP2_INM1 LCD_COM5/SEG16
									TIM1_CH2	
									USART1_RTS	

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									USART2_RTS	
									EVENTOUT	
									USART3_RTS	
-	-	27	4	40	PB4	I/O	COM_L		SPI1_MISO/I2S1_MCK	OPA2_OUT COMP2_INP1 LCD_COM6/SEG15
									TIM2_CH1	
									USART2_CTS	
									USART1_CTS	
									TIM17_BKIN	
									EVENTOUT	
									USART3_CTS	
-	18	28		41	PB5	I/O	COM_L		SPI1_MOSI/I2S1_SD	LCD_COM7/SEG14
									TIM2_CH2	
									TIM16_BKIN	
									USART2_CK	
									USART1_CK	
									COMP1_OUT	
									USART3_CK	
									TIM1_CH1	
8	-	29	6	42	PB6	I/O	COM_FL		USART1_TX	COMP2_INP0 LCD_SEG13
									TIM1_CH3	
									TIM16_CH1N	
									USART2_TX	
									SPI2_MISO	
									I2C1_SCL	

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									EVENTOUT	
									I2C2_SCL	
-	-	30		43	PB7	I/O	COM_FL		USART1_RX	PVD_IN COMP2_INM0 LCD_SEG12
									SPI2_MOSI	
									TIM17_CH1N	
									USART2_RX	
									I2C1_SDA	
									EVENTOUT	
									I2C2_SDA	
									TIM1_CH2	
-	19	31	7	44	PF7-BOOT0	I/O	COM	(3)	-	BOOT0
8	-	32		45	PB8	I/O	COM_F		SPI2_SCK	COMP1_INP0
									TIM16_CH1	
									I2C1_SCL	
									I2C2_SCL	
									USART2_TX	
									EVENTOUT	
									USART1_TX	
									SPI2_NSS	
									I2C1_SDA	
									I2C2_SDA	
									TIM17_CH1	
									IR_OUT	
-	-	-	-	46	PB9	I/O	COM		TIM17_CH1	-

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									EVENTOUT IROUT	
-	20	-	8	47	VSS	G	-		Ground	
1	1	1	9	48	V_{CC}	S	-		Digital power supply	

1. Configured by option bytes to choose PF2 or NRST.
2. After reset, PA13 and PA14 are configured as SWDIO and SWCLK AF functions, the former has an internal pull-up resistor and the latter has an internal pull-down resistor activated.
3. PF7-BOOT0 defaults to digital input mode and pull-down is enabled.

3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-3 Port A alternate functions mapping

Port A	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	SPI2_SCK	USART1_CTS			USART2_CTS			COMP1_OUT		USART2_TX	SPI1_MISO/ I2S1_MCK	USART3_CTS		TIM1_CH3	TIM1_CH1N	IR_OUT
PA1	SPI1_SCK/ I2S1_CK	USART1_RTS			USART2_RTS			EVENTOUT	USART3_RX	USART2_RX	SPI1_MOSI/ I2S1_SD	USART3_RTS		TIM1_CH4	TIM1_CH2N	MCO
PA2	SPI1_MOSI/ I2S1_SD	USART1_TX			USART2_TX			COMP2_OUT			SPI1_SCK/ I2S1_CK	I2C2_SDA	I2C1_SDA	TIM2_CH1		
PA3	SPI2_MISO	USART1_RX			USART2_RX			EVENTOUT			SPI1_MOSI/I 2S1_SD	I2C2_SCL	I2C1_SCL	TIM1_CH1		
PA4	SPI1_NSS/ I2S1_WS	USART1_CK	SPI2_MOSI		TIM14_CH1	USART2_CK		EVENTOUT	USART3_TX	USART2_TX				TIM2_CH3		RTC_OUT
PA5	SPI1_SCK/ I2S1_CK							EVENTOUT		USART2_RX				TIM2_CH2		MCO
PA6	SPI1_MISO/ I2S1_MCK	TIM2_CH1	TIM1_BKIN			TIM16_CH1		COMP1_OUT	USART1_CK							RTC_OUT
PA7	SPI1_MOSI/ I2S1_SD	TIM2_CH2	TIM1_CH1N		TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT	USART1_TX	USART2_TX	SPI1_MISO/ I2S1_MCK	I2C2_SDA	I2C1_SDA			
PA8	SPI2_NSS	USART1_CK	TIM1_CH1		USART2_CK	MCO		EVENTOUT	USART1_RX	USART2_RX	SPI1_MOSI/ I2S1_SD	I2C2_SCL	I2C1_SCL			
PA9	SPI2_MISO	USART1_TX	TIM1_CH2		USART2_TX	MCO	I2C1_SCL	EVENTOUT	USART1_RX		SPI1_SCK/ I2S1_CK	I2C2_SDA	I2C1_SDA	TIM1_BKIN		
PA10	SPI2_MOSI	USART1_RX	TIM1_CH3		USART2_RX	TIM17_BKIN	I2C1_SDA	EVENTOUT	USART1_TX		SPI1_NSS/ I2S1_WS	I2C2_SCL	I2C1_SCL			
PA11	SPI1_MISO/ I2S1_MCK	USART1_CTS	TIM1_CH4		USART2_CTS	EVENTOUT	I2C1_SCL	COMP1_OUT				I2C2_SCL				
PA12	SPI1_MOSI/ I2S1_SD	USART1_RTS	TIM1_ETR		USART2_RTS	EVENTOUT	I2C1_SDA	COMP2_OUT				I2C2_SDA				
PA13	SWDIO	IR_OUT						EVENTOUT	USART1_RX		SPI1_MISO/ I2S1_MCK			TIM1_CH2		MCO
PA14	SWCLK	USART1_TX			USART2_TX			EVENTOUT	USART3_TX		SPI1_SCK/ I2S1_CK					MCO
PA15	SPI1_NSS/ I2S1_WS	USART1_RX			USART2_RX			EVENTOUT	USART3_RX							

3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-4 Port B alternate function mapping

Port B	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	SPI1_NSS/ I2S1_WS	TIM2_CH3	TIM1_CH2N			EVENTOUT		COMP1_OUT				USART3_CK				
PB1	TIM14_CH1	TIM2_CH4	TIM1_CH3N					EVENTOUT				USART3_RTS				
PB2	USART1_RX		TIM1_CH2	USART2_RX					USART3_RX		SPI2_SCK					
PB3	SPI1_SCK/ I2S1_CK	TIM1_CH2		USART1_RTS	USART2_RTS			EVENTOUT	USART3_RTS							
PB4	SPI1_MISO/ I2S1_MCK	TIM2_CH1		USART1_CTS	USART2_CTS	TIM17_BKIN		EVENTOUT	USART3_CTS							
PB5	SPI1_MOSI/ I2S1_SD	TIM2_CH2	TIM16_BKIN	USART1_CK	USART2_CK			COMP1_OUT	USART3_CK					TIM1_CH1		
PB6	USART1_TX	TIM1_CH3	TIM16_CH1N	SPI2_MISO	USART2_TX		I2C1_SCL	EVENTOUT				I2C2_SCL				
PB7	USART1_RX	SPI2_MOSI	TIM17_CH1N		USART2_RX		I2C1_SDA	EVENTOUT				I2C2_SDA		TIM1_CH2		
PB8		SPI2_SCK	TIM16_CH1		USART2_TX	I2C2_SCL	I2C1_SCL	EVENTOUT	USART1_TX			SPI2_NSS	I2C1_SDA	TIM17_CH1	I2C2_SDA	IR_OUT
PB9			TIM17_CH1					EVENTOUT								IR_OUT
PB10	SPI2_SCK		TIM2_CH3	USART3_TX								I2C2_SCL	I2C1_SCL			
PB11			TIM2_CH4	USART3_RX				EVENTOUT				I2C2_SDA	I2C1_SDA			
PB12	SPI1_NSS/ I2S1_WS	SPI2_NSS	TIM1_BKIN					EVENTOUT				USART3_RTS		TIM1_BKIN		
PB13	SPI2_SCK		TIM1_CH1N								SPI1_SCK/ I2S1_CK	USART3_CTS				
PB14	SPI2_MISO		TIM1_CH2N								SPI1_MISO/ I2S1_MCK	USART3_RTS				
PB15	SPI2_MOSI		TIM1_CH3N								SPI1_MOSI/ I2S1_SD					

3.3. Alternate functions selected through GPIOF_AFR registers for port F

Table 3-5 Port F alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0			TIM14_CH1	SPI2_SCK	USART2_RX				USART1_RX	USART2_TX		I2C2_SDA	I2C1_SDA			
PF1				SPI2_MISO	USART2_TX				USART1_TX	USART2_RX	SPI1_NSS/ I2S1_WS	I2C2_SCL	I2C1_SCL	TIM14_CH1		
PF2		TIM2_CH2	TIM1_CH2	SPI2_MOSI	USART2_RX		MCO							TIM1_CH1N		
PF3	USART1_TX			SPI2_MISO	USART2_TX						SPI1_NSS/ I2S1_WS			TIM2_CH3		RTC_OUT
PF4																
PF5		IR_OUT						EVENTOUT	USART1_RX		SPI1_MISO / I2S1_MCK	I2C2_SCL	I2C2_SDA	TIM1_CH2		
PF6		USART1_TX	TIM1_CH2N		USART2_TX			EVENTOUT				I2C2_SDA	I2C2_SCL			
PF7																
PF8			TIM1_CH1	SPI2_MOSI	USART2_RX		MCO									
PF9		TIM2_CH1	TIM1_CH1N	SPI2_SCK	USART2_TX											
PF10																
PF11																

4. Memory mapping

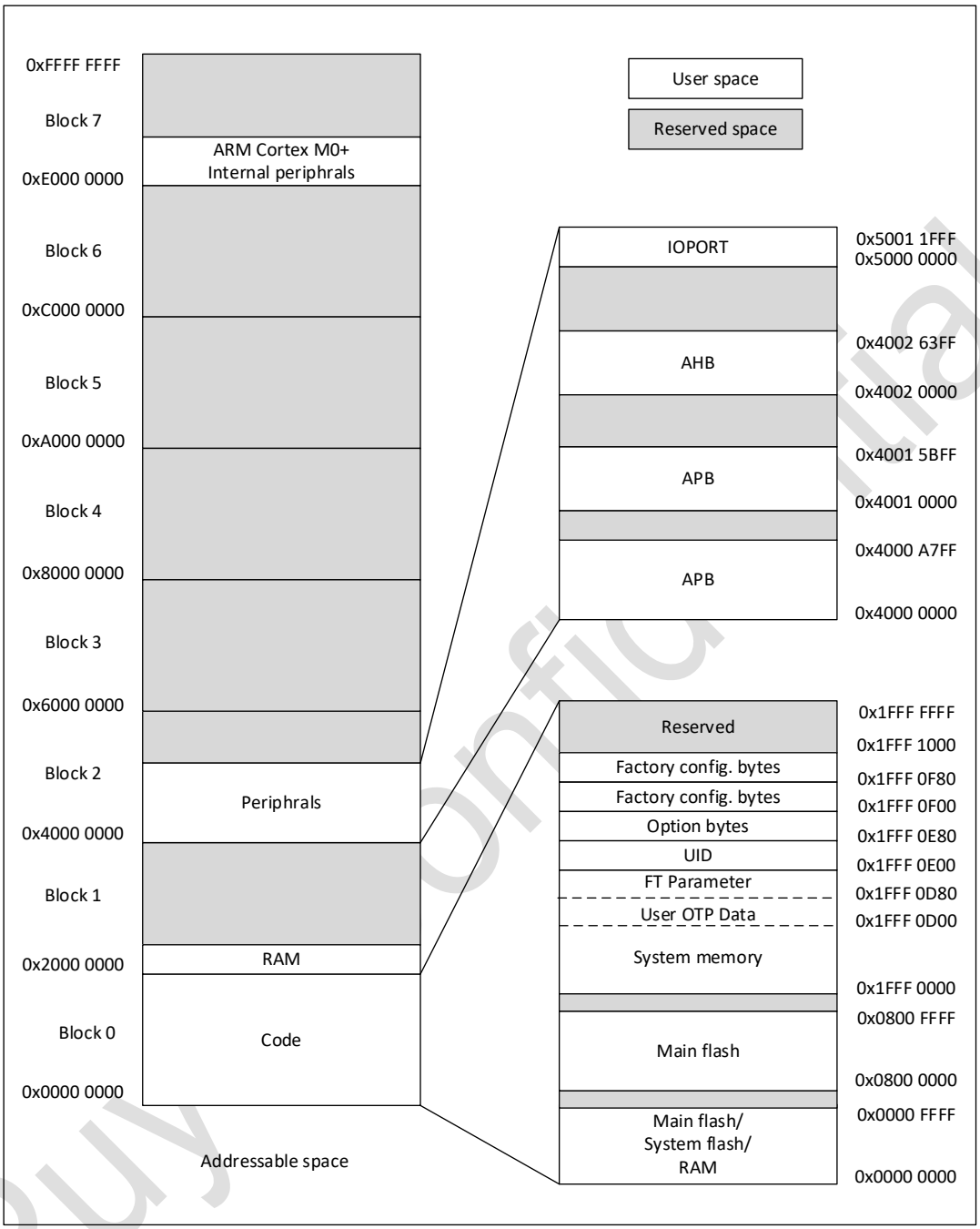


Figure 4-1 Memory mapping

Table 4-1 Memory boundary address

Type	Boundary Address	Size	Memory Area	Description
SRAM	0x2000 2000-0x3FFF FFFF	-	Reserved	-
	0x2000 0000-0x2000 1FFF	8 KB	SRAM	-
Code	0x1FFF 1000-0x1FFF FFFF	-	Reserved	-
	0x1FFF 0F80-0x1FFF 0FFF	128 Bytes	Factory config. bytes	-
	0x1FFF 0F00-0x1FFF 0F7F	128 Bytes	Factory config. bytes	Store HSI trimming data
	0x1FFF 0E80-0x1FFF 0EFF	128 Bytes	Option bytes	Option bytes information

Type	Boundary Address	Size	Memory Area	Description
	0x1FFF 0E00-0x1FFF 0E7F	128 Bytes	UID	Unique ID
	0x1FFF 0D80-0x1FFF 0DFF	-	Reserved	-
	0x1FFF 0D00-0x1FFF 0D7F	128 Bytes	User OTP Data	User OTP
	0x1FFF 0000-0x1FFF 0CFF	3.25 KB	System memory	Store Boot loader
	0x0801 0000-0x1FFE FFFF	-	Reserved	-
	0x0800 0000-0x0800 FFFF	64 KB	Main flash memory	-
	0x0001 0000-0x07FF FFFF	-	Reserved	-
	0x0000 0000-0x0000 FFFF	64 KB	Selection based on Boot configuration： 1) Main flash memory 2) System flash memory 3) SRAM	-

1. The address is marked as Reserved, which cannot be written, read as 0, and a response error is generated.

Table 4-2 Peripheral register address

Bus	Boundary Address	Size	Peripheral
	0xE000 000-0xE00F FFFF	1 MB	M0+
IOPORT	0x5000 1800-0x5FFF FFFF	-	Reserved
	0x5000 1400-0x5000 17FF	1 KB	GPIOF
	0x5000 1000-0x5000 13FF	-	Reserved
	0x5000 0C00-0x5000 0FFF	-	Reserved
	0x5000 0800-0x5000 0BFF	-	Reserved
	0x5000 0400-0x5000 07FF	1 KB	GPIOB
	0x5000 0000-0x5000 03FF	1 KB	GPIOA
AHB	0x4002 4000-0x4FFF FFFF	-	Reserved
	0x4002 3C00-0x4002 3FFF	-	Reserved
	0x4002 3800-0x4002 3BFF	1 KB	HDIV
	0x4002 3400-0x4002 37FF	1 KB	CORDIC
	0x4002 3000-0x4002 33FF	1 KB	CRC
	0x4002 2400-0x4002 2FFF	-	Reserved
	0x4002 2000-0x4002 23FF	1 KB	Flash
	0x4002 1C00-0x4002 1FFF	-	Reserved
	0x4002 1800-0x4002 1BFF	1 KB	EXTI
	0x4002 1400-0x4002 17FF	-	Reserved
	0x4002 1000-0x4002 13FF	1 KB	RCC
	0x4002 0400-0x4002 0FFF	-	Reserved
	0x4002 0000-0x4002 03FF	1 KB	DMA
APB	0x4001 5C00-0x4001 FFFF	-	Reserved
	0x4001 5800-0x4001 5BFF	1 KB	DBG
	0x4001 4C00-0x4001 57FF	-	Reserved
	0x4001 4800-0x4001 4BFF	1 KB	TIM17
	0x4001 4400-0x4001 47FF	1 KB	TIM16

Bus	Boundary Address	Size	Peripheral
	0x4001 3C00-0x4001 43FF	-	Reserved
	0x4001 3800-0x4001 3BFF	1 KB	USART1
	0x4001 3400-0x4001 37FF	-	Reserved
	0x4001 3000-0x4001 33FF	1 KB	SPI1
	0x4001 2C00-0x4001 2FFF	1 KB	TIM1
	0x4001 2800-0x4001 2BFF	-	Reserved
	0x4001 2400-0x4001 27FF	1KB	ADC
	0x4001 0400-0x4001 23FF	-	Reserved
	0x4001 0300-0x4001 03FF	1KB	OPA
	0x4001 0200-0x4001 02FF		COMP1 and COMP2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 B400-0x4000 FFFF	-	Reserved
	0x4000 B000-0x4000 B3FF	-	Reserved
	0x4000 8400-0x4000 AFFF	-	Reserved
	0x4000 8000-0x4000 83FF	-	Reserved
	0x4000 7C00-0x4000 7FFF	1 KB	LPTIM
	0x4000 7400-0x4000 7BFF	-	Reserved
	0x4000 7000-0x4000 73FF	1 KB	PWR
	0x4000 5C00-0x4000 6FFF	-	Reserved
	0x4000 5800-0x4000 5BFF	1 KB	I2C2
	0x4000 5400-0x4000 57FF	1 KB	I2C1
	0x4000 4C00-0x4000 53FF	-	Reserved
	0x4000 4800-0x4000 4BFF	1 KB	USART3
	0x4000 4400-0x4000 47FF	1 KB	USART2
	0x4000 3C00-0x4000 43FF	-	Reserved
	0x4000 3800-0x4000 3BFF	1 KB	SPI2
	0x4000 3400-0x4000 37FF	-	Reserved
	0x4000 3000-0x4000 33FF	1 KB	IWDG
	0x4000 2C00-0x4000 2FFF	1 KB	WWDG
	0x4000 2800-0x4000 2BFF	1 KB	RTC
	0x4000 2400-0x4000 27FF	1 KB	LCD
	0x4000 2000-0x4000 23FF	1 KB	TIM14
	0x4000 1800-0x4000 1FFF	-	Reserved
	0x4000 1400-0x4000 17FF	-	Reserved
	0x4000 1000-0x4000 13FF	-	Reserved
	0x4000 0800-0x4000 13FF	-	Reserved
	0x4000 0400-0x4000 07FF	-	Reserved
	0x4000 0000-0x4000 03FF	1 KB	TIM2

5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A =25 °C and T_A =$T_{A(max)}$ (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation.

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A =25°C and V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95 % of the devices have an error less than or equal to the value indicated (measured value ±2σ).

5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Descriptions	Min	Max	Unit
V_{CC}	External mains power supply	-0.3	6.25	V
V_{IN}	Input voltage of other pins	-0.3	V_{CC} + 0.3	V

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.

Table 5-2 Current characteristics

Symbol	Descriptions	Max	Unit
ΣI_{VCC}	Total current into sum of all V_{CC} power lines (source)(1)	150	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
$I_{IO(PIN)}$	Output current sunk by any COM I/O and control pin(2)	20	
	Output current sunk by any COM_L I/O and control pin(2)	80	
	Output current sourced by any I/O	-20	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.

Table 5-3 Thermal characteristics

Symbol	Descriptions	Conditions	Value	Unit
T_{STG}	Storage temperature range	-	-65 - +150	℃
T_O	Operating temperature range	x6 version	-40 - +85	℃
		x7 version	-40 - +105	

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK}	Internal APB clock frequency	-	0	72	MHz

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Standard operating voltage	-	1.7	5.5	V
V_{IN}	I/O input voltage	-	-0.3	V_{CC}+0.3	V
T_A	Ambient temperature	x6 version	-40	85	℃
		x7 version	-40	105	
T_J	Junction temperature	x6 version	-40	90	℃
		x7 version	-40	110	

5.3.2. Operating conditions at power-on / power-down

Table 5-5 Operating conditions at power-on / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise rate	-	0	∞	μs/V
	V_{CC} fall rate	-	30	∞	

5.3.3. Embedded reset and PVD module characteristics

Table 5-6 Embedded reset characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization	-	-	4.0	7.5	ms
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.53	1.63	1.70	V
		Falling edge	1.50	1.60	1.68	
V_{BOR1}	BOR1 threshold	Rising edge	1.70	1.80	1.90	V
		Falling edge	1.60	1.70	1.80	
V_{BOR2}	BOR2 threshold	Rising edge	1.90	2.00	2.10	V
		Falling edge	1.80	1.90	2.00	
V_{BOR3}	BOR3 threshold	Rising edge	2.10	2.20	2.30	V
		Falling edge	2.00	2.10	2.20	
V_{BOR4}	BOR4 threshold	Rising edge	2.30	2.40	2.50	V
		Falling edge	2.20	2.30	2.40	
V_{BOR5}	BOR5 threshold	Rising edge	2.50	2.60	2.70	V
		Falling edge	2.40	2.50	2.60	
V_{BOR6}	BOR6 threshold	Rising edge	2.70	2.80	2.90	V
		Falling edge	2.60	2.70	2.80	
V_{BOR7}	BOR7 threshold	Rising edge	2.90	3.00	3.10	V
		Falling edge	2.80	2.90	3.00	
V_{BOR8}	BOR8 threshold	Rising edge	3.10	3.20	3.30	V
		Falling edge	3.00	3.10	3.20	
V_{PVD0}	PVD0 threshold	Rising edge	1.74	1.84	1.94	V
		Falling edge	1.64	1.74	1.84	
V_{PVD1}	PVD1 threshold	Rising edge	1.94	2.04	2.14	V
		Falling edge	1.84	1.94	2.04	
V_{PVD2}	PVD2 threshold	Rising edge	2.12	2.22	2.32	V
		Falling edge	2.02	2.12	2.22	
V_{PVD3}	PVD3 threshold	Rising edge	2.32	2.42	2.52	V
		Falling edge	2.22	2.32	2.42	
V_{PVD4}	PVD4 threshold	Rising edge	2.55	2.65	2.75	V
		Falling edge	2.45	2.55	2.65	
V_{PVD5}	PVD5 threshold	Rising edge	2.75	2.85	2.95	V
		Falling edge	2.65	2.75	2.85	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD6 threshold	Rising edge	2.95	3.05	3.15	V
		Falling edge	2.85	2.95	3.05	
V_{PVD7}	PVD7 threshold	Rising edge	3.15	3.25	3.35	V
		Falling edge	3.05	3.15	3.25	
$V_{POR\_PDR\_hyst}$(1)	POR/PDR hysteresis	-	-	30	-	mV
$V_{PVD\_BOR\_hyst}$(1)	PVD hysteresis	-	-	100	-	mV
$I_{CC\ (PVD)}$ (1)	PVD power consumption	-	-	0.6	-	μA
$I_{CC\ (BOR)}$ (1)	BOR consumption	-	-	0.6	-	μA

1. Guaranteed by design, not tested in production.

5.3.4. Supply current characteristics

Table 5-7 Current consumption in Run mode

Symbol	Conditions						Typ(1)	Max	Unit
	System clock	Frequency	Code	Run	Peripheral Clock	Flash sleep			
I_{CC} (Run)	PLL (x3)	72 MHz	While(1)	Flash	ON	DISABLE	6.10	-	mA
					OFF	DISABLE	4.40	-	
	PLL (x2)	48 MHz			ON	DISABLE	5.00	-	
					OFF	DISABLE	3.80	-	
	HSI	24 MHz			ON	DISABLE	2.80	-	
					OFF	DISABLE	2.20	-	
		16 MHz			ON	DISABLE	2.00	-	
					OFF	DISABLE	1.60	-	
		8 MHz			ON	DISABLE	1.20	-	
					OFF	DISABLE	1.00	-	
		4 MHz			ON	DISABLE	0.80	-	
					OFF	DISABLE	0.60	-	
	LSI	32.768 kHz			ON	DISABLE	180	-	μA
					OFF	DISABLE	180	-	
		32.768 kHz			ON	ENABLE	135	-	
					OFF	ENABLE	135	-	

1. Data based on characterization results, not tested in production.

Table 5- 8 Current consumption in Sleep mode

Symbol	Conditions				Typ(1)	Max	Unit
	System clock	Frequency	Peripheral Clock	Flash sleep			
I_{CC}(sleep)	PLL (x3)	72 MHz	ON	DISABLE	4.60	-	mA
			OFF	DISABLE	2.50	-	
	PLL (x2)	48 MHz	ON	DISABLE	3.50	-	
			OFF	DISABLE	2.10	-	
	HSI	24 MHz	ON	DISABLE	1.80	-	
			OFF	DISABLE	1.00	-	
		16 MHz	ON	DISABLE	1.30	-	
			OFF	DISABLE	0.80	-	
		8 MHz	ON	DISABLE	0.80	-	
			OFF	DISABLE	0.50	-	
		4 MHz	ON	DISABLE	0.50	-	
			OFF	DISABLE	0.40	-	
	LSI	32.768 kHz	ON	DISABLE	180	-	μA

	Conditions						
			OFF	DISABLE	178	-	
		32.768 kHz	ON	ENABLE	95.0	-	
			OFF	ENABLE	95.0	-	

1. Data based on characterization results, not tested in production.

Table 5-9 Current consumption in Stop mode

Symbol	Conditions				Typ(1)	Max	Unit
	V_{CC}	LDO mode	LSI	Peripheral Clock			
I_{CC}(Stop)	1.7 - 5.5 V	MR	-	-	85.0	-	μA
		LPR	ON	RTC+IWDG+LPTIM	4.50	-	
				IWDG	4.30	-	
				LPTIM	4.30	-	
				RTC	4.30	-	
			OFF	No	4.00	-	

1. Data based on characterization results, not tested in production.

5.3.5. Wakeup time from low-power mode

Table 5 -10 Wake-up time from low-power mode

Symbol	Parameter(1)	LDO mode	Conditions	Typ(2)	Max	Unit
$t_{WMSLEEP}$	Wake-up from Sleep mode	MR	Run program in Flash	4.0	-	CPU Cycles
t_{WUSTOP}	Wake-up from Stop mode	MR	Run program in Flash HSI (24 MHz) as system clock FLS_SLPTI[1:0] = 00	6.5	-	μs
		LPR	Run program in Flash HSI (24 MHz) as system clock FLS_SLPTI[1:0] = 00	10.2	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data based on characterization results, not tested in production.

5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the device stops working, the corresponding I/O is used as a standard GPIO.

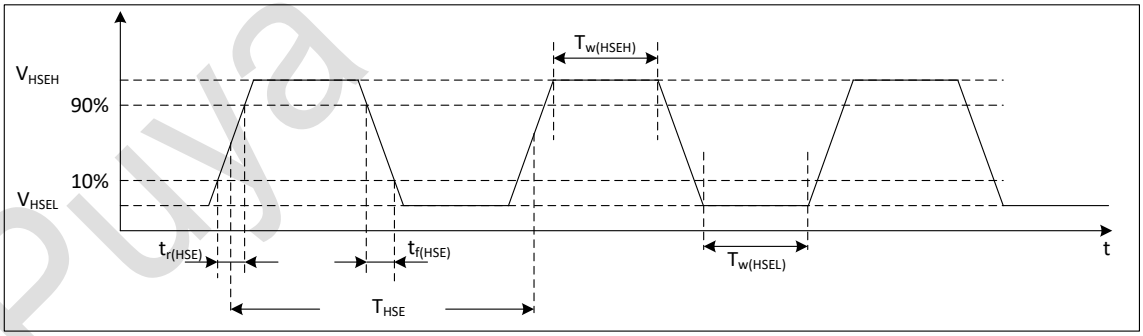


Figure 5-1 High-speed external clock timing diagram

Table 5-11 High-speed external clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	1	8	32	MHz
V_{HSEH}	Input pin high level voltage	0.7*V_{CC}	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	Vss	-	0.3*V_{CC}	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	High or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Rise or fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

5.3.6.2. Low-speed external clock generated from an external source

In the bypass mode of LSE (the LSEBYP of RCC_BDCR is set), the low-speed start-up circuit in the chip stops working, and the corresponding I/O is used as a standard GPIO.

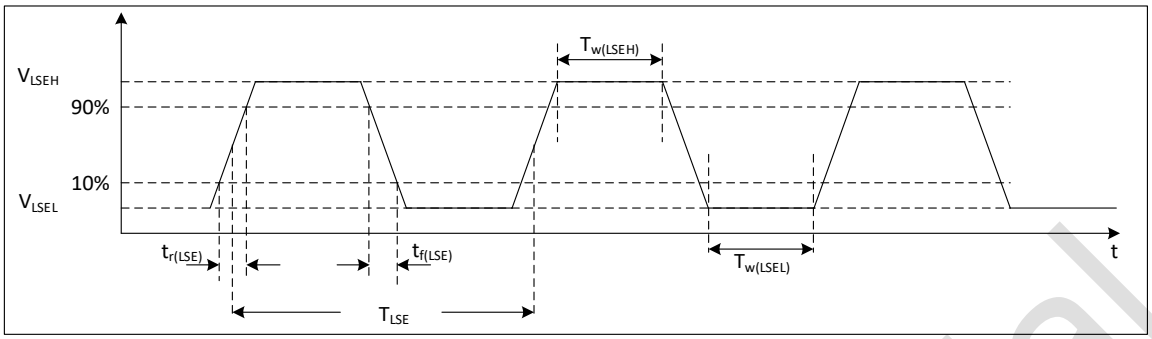


Figure 5-2 Low-speed external clock timing diagram

Table 5-12 Low-speed external clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	32.768	1000	kHz
V_{LSEH}	Input pin high level voltage	0.7*V_{CC}	-	-	V
V_{LSEL}	Input pin low level voltage	-	-	0.3*V_{CC}	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	High or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Rise or fall time	-	-	50	ns

1. Guaranteed by design, not tested in production.

5.3.6.3. High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with 4 -32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-13 HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
I_{CC}(4)	HSE current consumption	Startup time	-	-	5.5	mA
		V_{CC}=3 V, R_m=30 Ω, C_L=10 pF@8 MHz HSE_DRV [1:0] = 01	-	0.58	-	
		V_{CC}=3 V, R_m=30 Ω, CL=5 pF@16 MHz HSE_DRV [1:0] = 10	-	0.89	-	
		V_{CC}=3 V, R_m=30 Ω, C_L=10 pF@24 MHz HSE_DRV [1:0] = 10/11	-	1.14	-	
		V_{CC}=3 V, R_m=30 Ω, C_L=20 pF@32 MHz HSE_DRV [1:0] = 11	-	1.94	-	
$t_{SU(HSE)}$(3)(4)	Startup time	f_{OSC_IN}= 32 MHz LSE_STARTUP [1:0] = 00 HSE_DRV [1:0] = 11	-	0.3	-	ms
		f_{OSC_IN}= 4 MHz LSE_STARTUP [1:0] = 00 HSE_DRV [1:0] = 11	-	1.6	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.

3. $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state, measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another.
4. Data based on characterization results, not tested in production.

5.3.6.4. Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-14 LSE oscillator characteristics

Symbol	Parameter	Conditions (1)	Min(2)	Typ	Max(2)	Unit
I_{CC}(4)	LSE current consumption	LSE_DRIVER [1:0] = 00	-	-	-	nA
		LSE_DRIVER [1:0] = 01	-	560	-	
		LSE_DRIVER [1:0] = 10	-	920	-	
		LSE_DRIVER [1:0] = 11	-	1260	-	
$t_{SU(LSE)}$(3)(4)	Startup time	LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 11	-	400	-	ms

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable, measured for a standard crystal/resonator, which may vary greatly from crystal to resonator.
4. Data based on characterization results, not tested in production.

5.3.7. High-speed internal (HSI) RC oscillator

Table 5-15 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	T_A= 25 °C, V_{CC}= 3.3 V	23.83	24	24.17	MHz
			21.97	22.12	22.27	
			15.89	16	16.11	
			7.94	8	8.06	
			3.97	4	4.03	
$\Delta_{Temp(HSI)}$	HSI frequency drift over temperature	T_A = 25 ℃	-1(2)	-	1(2)	%
		T_A = 0 - 85 ℃	-2(2)	-	2(2)	
		T_A = - 40 - 105 ℃	-3(2)	-	3.5(2)	
f_{TRIM}(1)	HSI trimming accuracy	-	-	0.1	-	%
D_{HSI}(1)	Duty cycle	-	45(1)	-	55(1)	%
$t_{Stab(HSI)}$	HSI stabilization time	-	-	2	4(1)	μs
$I_{CC(HSI)}$(2)	HSI power consumption	4 MHz	-	120	-	μA
		8 MHz	-	150	-	
		16 MHz	-	250	-	
		22.12 MHz, 24 MHz	-	350	-	

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.8. Low-speed internal (LSI) RC oscillator

Table 5-16 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	T_A= 25 °C, V_{CC}= 3.3 V	-3	-	3	%
$\Delta_{Temp(LSI)}$	LSI frequency drift over temperature	T_A=0 - 85 °C	-10(2)	-	10(2)	%
		T_A= -40 - 105 °C	-18(2)	-	18(2)	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIM}(1)	LSI trimming accuracy	-	-	0.2	-	%
$t_{Stab(LSI)}$ (1)	LSI stabilization time	-	-	150	-	μs
$ICC_{(LSI)}$(1)	LSI power consumption	-	-	300	-	nA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.9. Phase locked loop (PLL) characteristics

Table 5-17 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	T_A=25 °C, V_{CC}=3.3 V, PLL *2	16(1)	-	24(1)	MHz
		T_A=25 °C, V_{CC}=3.3 V, PLL *3	22(1)	-	24(1)	
f_{PLL_OUT}	PLL output clock	TA=25 °C, V_{CC}=3.3 V	32(1)	-	72	MHz
Jitter	Period jitter	-	-	-	0.3(1)	ns
t_{LOCK}	PLL lock time	f_{PLL_IN}=24 MHz	-	15	40(1)	μs

1. Guaranteed by design, not tested in production.

5.3.10. Memory characteristics

Table 5-18 Memory characteristics

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}	Page programming time	-	1.5	2.0	ms
t_{ERASE}	Page/sector/mass erase time	-	3.5	4.5	ms
I_{CC}	Page programming supply current	-	2.1	2.9	mA
	Page/sector/mass erase supply current	-	2.1	2.9	

1. Guaranteed by design, not tested in production.

Table 5-19 Memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 - 85 ℃	100	kcycle
		T_A = 85 - 105 ℃	10	
t_{RET}	Data retention time	10 kcycle T_A = 55 ℃	20	Year

1. Data based on characterization results, not tested in production.

5.3.11. EFT characteristics

Table 5-20 EFT characteristics

Symbol	Parameter	Conditions	Grade
EFT to Power	-	IEC61000-4-4	4 A

5.3.12. ESD & LU characteristics

Table 5-21 ESD&LU characteristics

Symbol	Parameter	Conditions	Typ	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	8	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	ESDA/JEDEC JS-002-2018	2	kV
LU	Static latch-up	JESD78E	200	mA

5.3.13. I/O port characteristics

Table 5-22 IO static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{CC}= 1.7 - 5.5 V	0.7 V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC}= 1.7 - 5.5 V	-	-	0.3V_{CC}	V
V_{hys}(1)	Schmitt trigger hysteresis	-	-	200	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	-	30	50	70	kΩ
R_{PD}	Weak pull-down equivalent resistor	-	30	50	70	kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IO}(1)	Pin capacitance	-	-	5	-	pF

1. Guaranteed by design, not tested in production.

Table 5-23 Output voltage characteristics(4)

Symbol	Parameter(3)	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level for a COM IO pin	I_{OL} = 20 mA, V_{CC} ≥ 5.0 V	-	0.6	V
		I_{OL} = 8 mA, V_{CC} ≥ 2.7 V - 0.4 V	-	0.4	
		I_{OL} = 4 mA, V_{CC} = 1.8 V - 0.5	-	0.5	
	Output low level voltage for an I/O pin(COM_L)(2)	I_{OL} = 10 mA, V_{CC} = 1.8 V	-	0.5	
		I_{OL} = 20 mA, V_{CC} ≥ 2.7 V		0.6	
		I_{OL} = 20 mA, V_{CC} ≥ 3.3V	-	0.5	
		I_{OL} = 20 mA, V_{CC} = 1.8 V	-	0.5	
		I_{OL} = 40 mA, V_{CC} ≥ 2.7 V	-	0.6	
		I_{OL} = 40 mA, V_{CC} ≥ 3.3 V	-	0.5	
		I_{OL} = 30 mA, V_{CC} = 1.8 V	-	0.5	
		I_{OL} = 60 mA, V_{CC} ≥ 2.7 V	-	0.6	
		I_{OL} = 60 mA, V_{CC} ≥ 3.3 V	-	0.5	
		I_{OL} = 40 mA, V_{CC} = 1.8 V	-	0.5	
		I_{OL} = 80 mA, V_{CC} ≥ 2.7 V	-	0.8	
		I_{OL} = 80 mA, V_{CC} ≥ 3.3 V	-	0.7	
V_{OH}(1)	Output high level voltage for an I/O pin	I_{OH} = 20 mA, V_{CC} ≥ 5.0 V	V_{CC}–0.6	-	V
		I_{OH} = 8 mA, V_{CC} ≥ 2.7 V	V_{CC}–0.4	-	
		I_{OH} = 4 mA, V_{CC} = 1.8 V	V_{CC}–0.5	-	

1. These I/O types refer to the terms and symbols defined by pins.
2. COM_L IO current (80 mA/60 mA/40 mA/20 mA) can be set by software.
3. Data based on characterization results, not tested in production.
4. The combined maximum current across all output pins (including contributions from both V_{OL} and V_{OH} states) must not exceed the $\Sigma I_{IO(PIN)}$ maximum rating specified in Table 5-2 Current characteristics.

5.3.14. NRST pin characteristics

Table5-24 NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{CC}=1.7 - 5.5 V	0.7V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC}=1.7 - 5.5 V	-	-	0.2V_{CC}	V
V_{hys}(1)	Schmitt trigger hysteresis	-	-	300	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}(1)	Weak pull-up equivalent resistor	-	30	50	70	kΩ
R_{PD}(1)	Weak pull-down equivalent resistor	-	30	50	70	kΩ
C_{IO}	Pin capacitance	-	-	5	-	pF

1. Guaranteed by design, not tested in production.

5.3.15. ADC characteristics

Table 5-25 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	1.7	-	5.5	V
I_{CC} (1)	Consumption	f_s =1 Msps	-	1.0	-	mA
C_{IN}(1)	Internal sampling and holding capacitor	-	-	5	-	pF
f_{ADC}	ADC clock frequency	V_{CC} = 1.7 - 2.3 V	0.8	4	8(2)	MHz
		V_{CC} = 2.3 - 5.5 V	0.8	8	16(2)	
t_{samp}(1)	Sampling time	V_{CC} = 1.7 - 5.5 V	3.5	-	239.5	1/f_{ADC}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{samp_setup}(1)	Sampling time for internal channels (V_{REFINT}，V_{CC}/3，OPA1_OUT，OPA2_OUT)	-	20	-	-	μs
t_{conv}(1)	Total conversion time	-	-	12	-	$1/f_{ADC}$
t_{eoc}(1)	Conversion end time	-	-	0.5	-	$1/f_{ADC}$

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

Table5-26 ADC accuracy

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.7 V < V_{CC} <2.3 V, fs =0.5 Msps, T_A = entire range	-	4	5	LSB
		2.3 V ≤ V_{CC} <5.5 V, fs =1 Msps, T_A = entire range	-	3	5	
EO	Offset error	1.7 V < V_{CC} <5.5 V, T_A = entire range	-	2	3	LSB
EG	Gain error	1.7 V < V_{CC} <5.5 V, T_A = entire range	-	4	8	LSB
ED	Differential linearity error	1.7 V < V_{CC} <2.3 V, fs =0.5 Msps, T_A = entire range	-	4	5	LSB
		2.3 V ≤ V_{CC} <5.5 V, fs =1 Msps, T_A = entire range		2	3	
EL	Differential linearity error	1.7 V < V_{CC} <2.3 V, fs =0.5 Msps, T_A = entire range	-	3	5	LSB
		2.3 V ≤ V_{CC} <5.5 V, fs =1 Msps, T_A = entire range		2	4	

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.16. Comparator characteristics

Table 5-27 Comparator characteris(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	Supply voltage	-		1.7	-	5.5	V
V_{IN}	Input voltage range	-		0	-	V_{CC}	V
t_{START}	Startup time	High-speed mode		-	-	5	μs
		Medium-speed mode		-	-	15	
t_D	Propagation delay	High-speed mode	200 mV step 100 mV over-drive	-	40	70	ns
			>200 mV step 100 mV over-drive	-	-	85	
		Medium-speed mode	200 mV step 100 mV over-drive	-	0.9	2.3	μs
			>200 mV step 100 mV over-drive	-	-	3.4	
V_{offset}	Offset voltage	-		-	±5	-	mV
V_{hys}	Hysteresis voltage	No hysteresis		-	0	-	mV
		With hysteresis		-	20	-	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	Operating current	High-speed mode	Static	-	250	400	μA
			With 50 kHz and ±100 mv overdrive square signal	-	250	-	
		Medium-speed mode	Static	-	5	7.5	
			With 50 kHz and ±100 mv overdrive square signal	-	6	-	
I_{sleep}	Sleep power consumption	-	-	-	1	-	nA

1. Guaranteed by design, not tested in production.

5.3.17. Operational amplifier characteristics

Table 5-28 Operational amplifier characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	2.2	-	5.5	V
V_i	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0.1	-	V_{CC}-0.2	V
I_O	Output current	-	-	-	2.2	mA
R_L	Load resistor	-	5	-	-	kΩ
t_{start}	Initialization time	-	-	-	20	μs
V_{IO}	Input offset voltage	R_L=5 kΩ, C_L=25 pF	-	±8	-	mV
PM	Phase margin	V_{CC} = 3.3V, V_i = V_O = V_{CC} / 2, R_L=5 kΩ, C_L=25 pF	-	80(1)	-	Deg
UGBW	Unit gain bandwidth	V_{CC} = 3.3 V, V_i = V_O = V_{CC} / 2, R_L=5 kΩ, C_L=25 pF	-	5(1)	-	MHz
SR	Slew rate	R_L=5 kΩ, C_L=25 pF	-	8	-	V/μs

1. Guaranteed by design, not tested in production.

5.3.18. Temperature sensor characteristics

Table5-29 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	℃
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/℃
V_{30}	Voltage at 30 °C (±5 °C)	0.742	0.76	0.785	V
t_{START}(1)	Start up time entering in continuous mode	-	70	120	μs
t_{samp_setup} (1)	ADC sampling time when reading the temperature	20	-	-	μs

1. Guaranteed by design, not tested in production.

5.3.19. LCD Controller Characteristics

Table5-30 LCD Controller Characteristics

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
I_{LCD}(1)(3)	LCD supply current	External resistor drive mode	-	0.6	-	μA
		Internal low drive resistive mode	-	4	-	
		Internal middle drive resistive mode	-	7.5	-	
		Internal high drive resistive mode	-	10	-	
R_H(2)	Low drive resistance	-	-	1080	-	kΩ
R_M(2)	Middle drive resistance	-	-	540	-	
R_L(2)	High drive resistance	-	-	360	-	
V_{LCDH}	LCD adjustable highest level voltage	-	-	V_{CCA}	-	V

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{LCD3}	LCD highest level voltage	-	-	V_{LCDH}	-	
V_{LCD2}	LCD 2/3 level voltage	-	-	2/3 V_{LCDH}	-	
V_{LCD1}	LCD 1/3 level voltage	-	-	1/3 V_{LCDH}	-	
V_{LCD0}	LCD lowest level voltage	-	-	V_{SS}	-	
ΔV_{LCD}(3)	LCD voltage deviation	TA = -40 - 105 °C	-	-	±50	mV

1. LCD enabled with V_{CC}=3.3 V, 1/4 duty, 1/3 bias, scan frequency 256 Hz, all pixels active, no LCD connected.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

5.3.20. Embedded voltage reference characteristics

Table5-31 Embedded internal voltage reference (V_{REFINT}) characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$t_{start\_VREFINT}$	Start time of V_{REFINT}	-	10	15	μs
$T_{coeff\_VREFINT}$	Temperature coefficient of V_{REFINT}	-	-	100	ppm/℃
I_{CC}	V_{REFINT} consumption from V_{CC}	-	12	20	μA

1. Guaranteed by design, not tested in production.

5.3.21. ADC voltage reference buffer (V_{REFBUF})

Table 5-32 ADC voltage reference buffer (V_{REFBUF}) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REF25}	2.5 V internal reference bufferInternal reference voltage	T_A= 25 °C, V_{CC}=3.3 V	2.475	2.500	2.525	V
V_{REF20}	2.048 V internal reference buffer	T_A= 25 °C, V_{CC}=3.3 V	2.027	2.048	2.068	V
V_{REF15}	1.5 V internal reference buffer	T_A= 25 °C, V_{CC}=3.3 V	1.485	1.500	1.515	V
V_{REF10}	1.024 V internal reference bufferInternal reference voltage	T_A= 25 °C, V_{CC}=3.3 V	1.014	1.024	1.034	V
T_{coeff}(1)	Temperature coefficient of V_{REFBUF}	T_A = -40 - 105 °C	-	-	120	ppm/°C

5.3.22. Timer characteristics

Table 5-33 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.888	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 72 MHz	-	36	
Res_{TIM}	Timer resolution time	TIM1/14/16/17	-	16	bit
$t_{COUNTER}$	16-bit counter internal clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.013888	910	μs

Table 5-34 LPTIM characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PRESC[2:0]	Min	Max	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.946	
/8	3	0.2441	15997.338	
/16	4	0.4883	32001.229	

Prescaler	PRESC[2:0]	Min	Max	Unit
/32	5	0.9766	64002.458	
/64	6	1.9531	127998.362	
/128	7	3.9063	256003.277	

Table 5-35 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 5-36 WWDG characteristics (timeout period at 72 MHz PCLK)

Prescaler	WDGTB[1:0]	Min	Max	Unit
1*4096	0	0.057	3.641	ms
2*4096	1	0.114	7.282	
4*4096	2	0.228	14.564	
8*4096	3	0.455	29.127	

5.4. Communication interfaces

5.4.1.1. I²Cinterface characteristics

I²C interface meets the requirements of the I²C bus specification and reference manual:

- Standard-mode (Sm): 100 kHz
- Fast-mode (Fm): 400 kHz
- Fast-mode plus (Fm+): 1 MHz

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-37 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

5.4.1.2. SPI characteristics

Table 5-38 SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Full-duplex mode	Transmit only or receive only	-	36	MHz
			Simultaneous transmit and receive	-	24	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF		-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode		2Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode		2Tpclk	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Slave mode, presc = 2		Tpclk - 2	Tpclk + 1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode		1	-	ns
		Slave mode		3	-	
$t_{h(MI)}$	Data input hold time	Master mode		5	-	ns
$t_{h(SI)}$		Slave mode		2	-	
$t_{a(SO)}$	Data output access time	Slave mode		0	3Tpclk	ns
$t_{dis(SO)}$	Data output access time	Slave mode		2Tpclk	-	ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	0	20	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	2	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	1	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

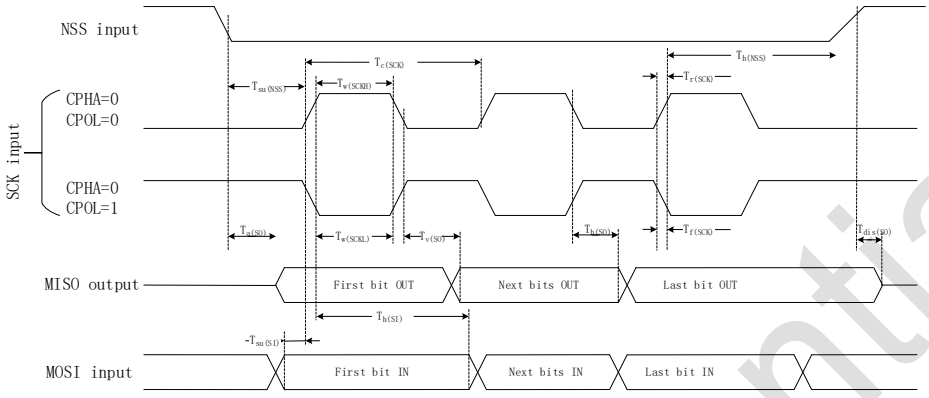


Figure 5-3 SPI timing diagram – Slave Mode and CPHA=0

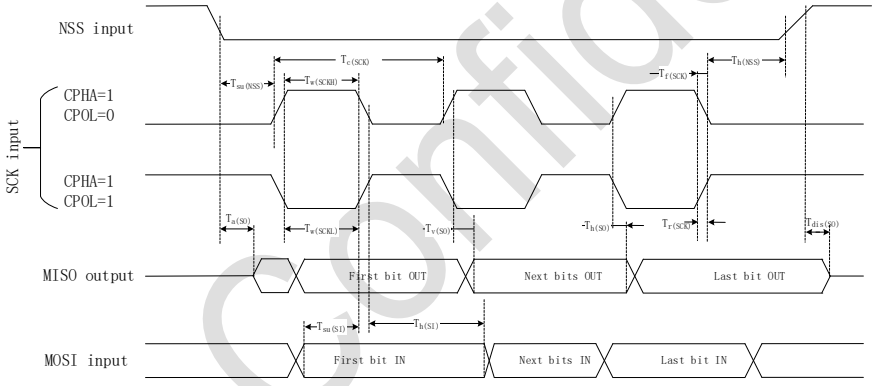


Figure 5-4 SPI timing diagram – Slave Mode and CPHA=1

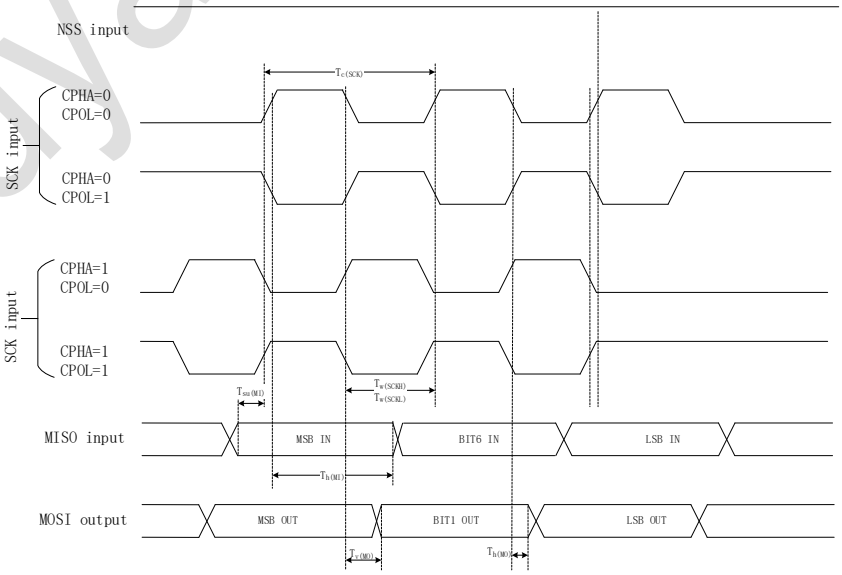
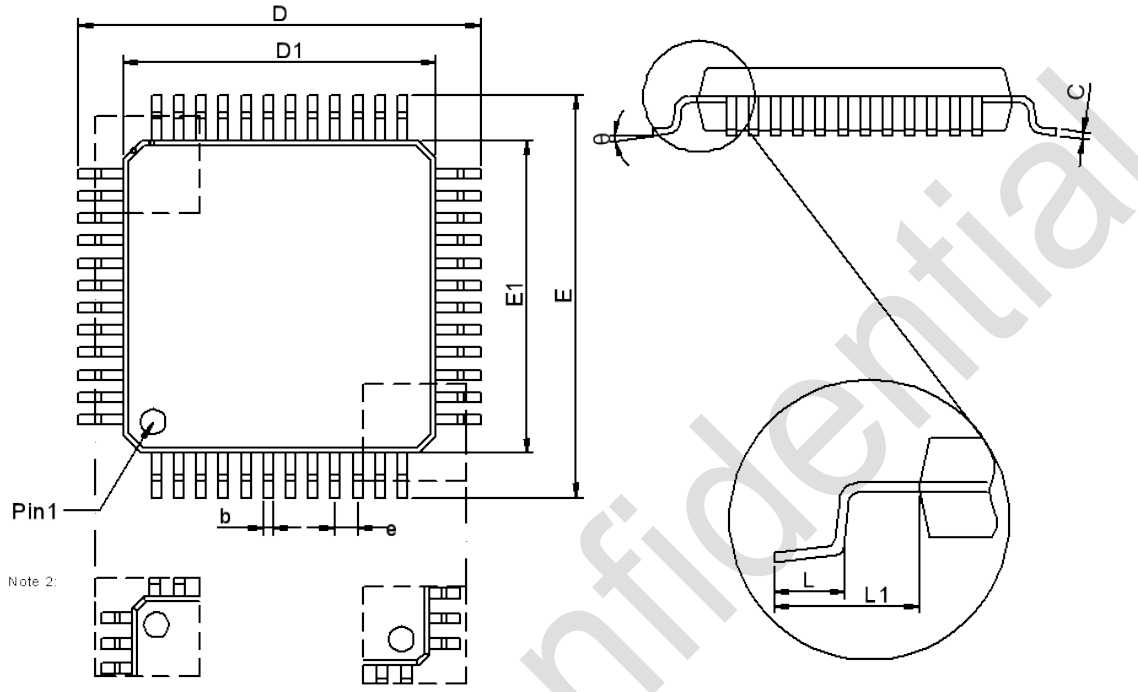


Figure 5-5 SPI timing diagram–Master mode

6. Package information

6.1. LQFP48 package size



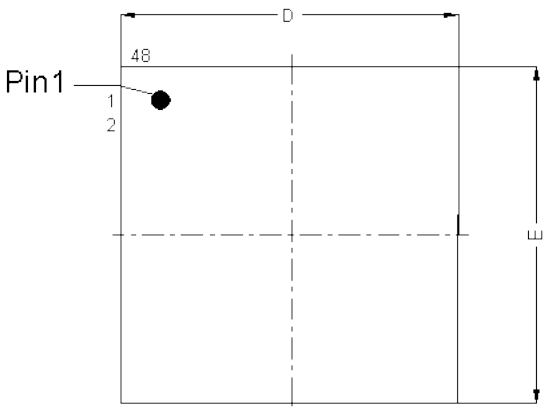
Common Dimensions
(Unit of Measure=millimeters)

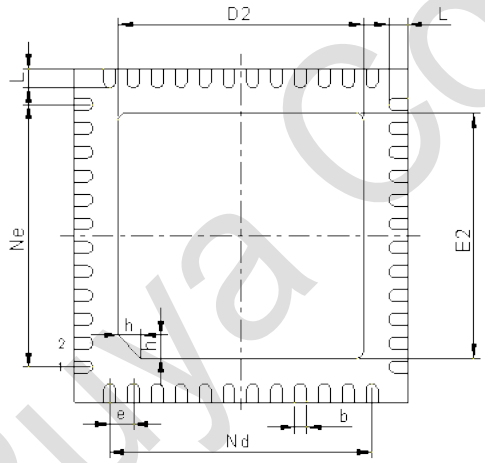
Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	8.800	9.000	9.200
D1	6.900	7.000	7.100
E	8.800	9.000	9.200
E1	6.900	7.000	7.100
e		0.500BSC	
L	0.450	-	0.750
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP48L 7x7X1.4-0.5PITCH	QRPD-0050	1.1

6.2. QFN48 (6*6) Package





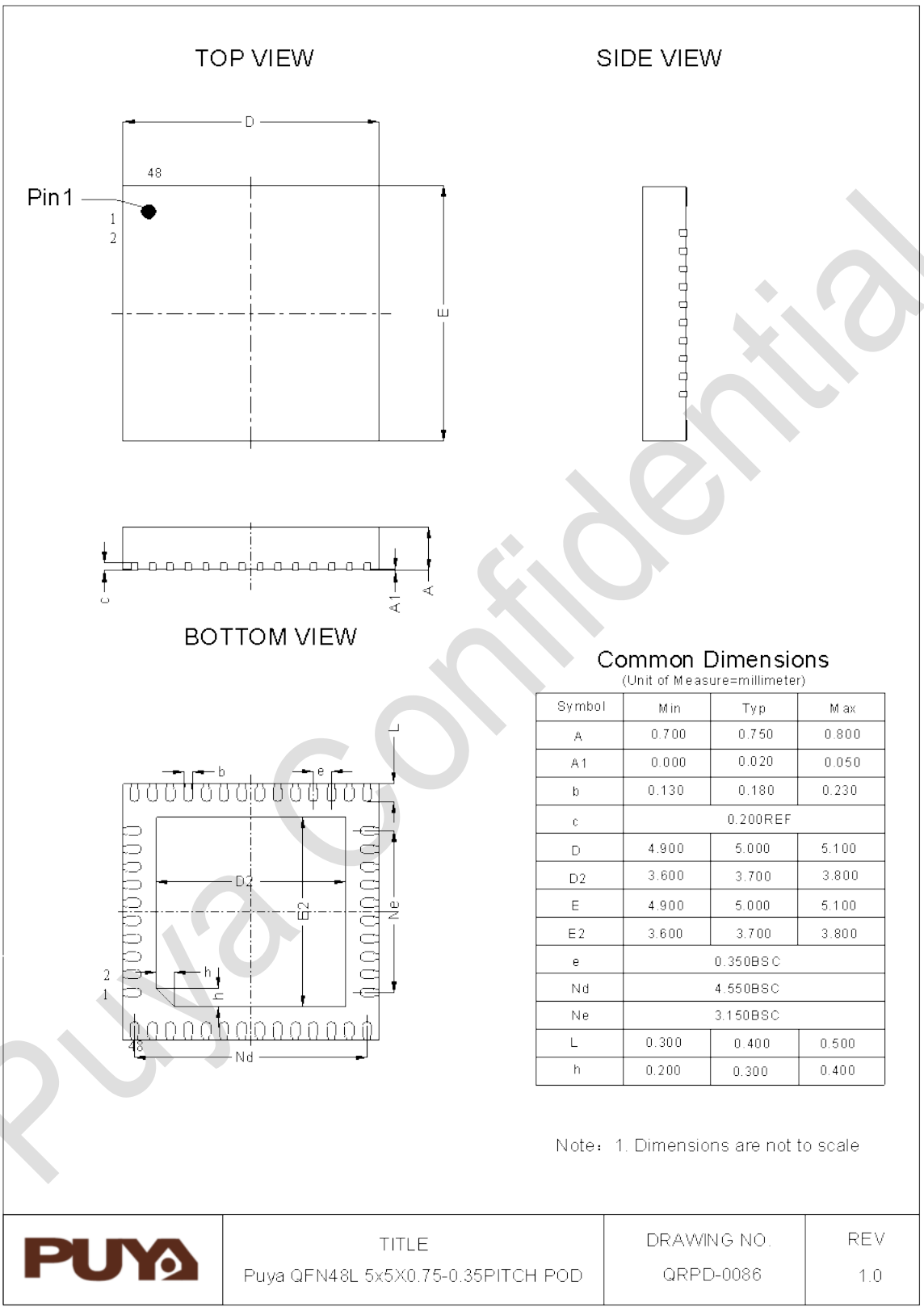
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c		0.200REF	
D	5.900	6.000	6.100
D2	4.100	4.300	4.500
E	5.900	6.000	6.100
E2	4.100	4.300	4.500
e		0.400BSC	
Nd		4.400BSC	
Ne		4.400BSC	
L	0.300	0.400	0.500
h	0.300	0.350	0.400

Note: 1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN48L 6X6X0.75-0.4PITCH POD	QRPD-0056	1.1

6.3. QFN48 (5*5) Package



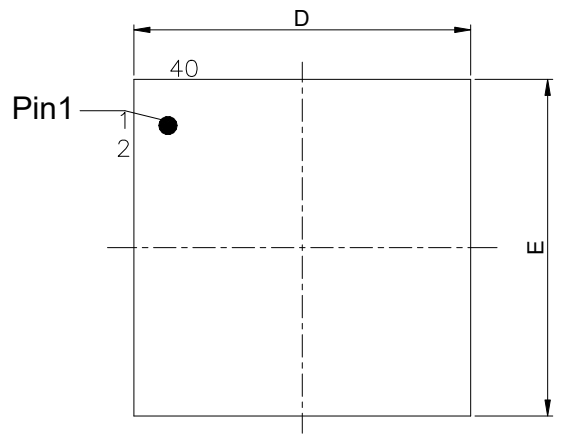
Common Dimensions
(Unit of Measure=millimeter)

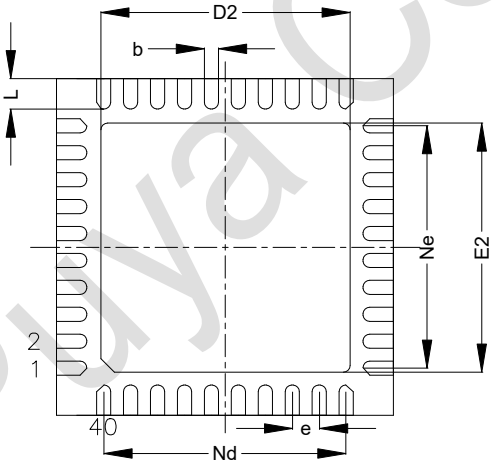
Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.130	0.180	0.230
c		0.200REF	
D	4.900	5.000	5.100
D2	3.600	3.700	3.800
E	4.900	5.000	5.100
E2	3.600	3.700	3.800
e		0.350BSC	
Nd		4.550BSC	
Ne		3.150BSC	
L	0.300	0.400	0.500
h	0.200	0.300	0.400

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN48L 5x5X0.75-0.35PITCH POD	QRPD-0086	1.0

6.4. QFN40 package size





Common Dimensions

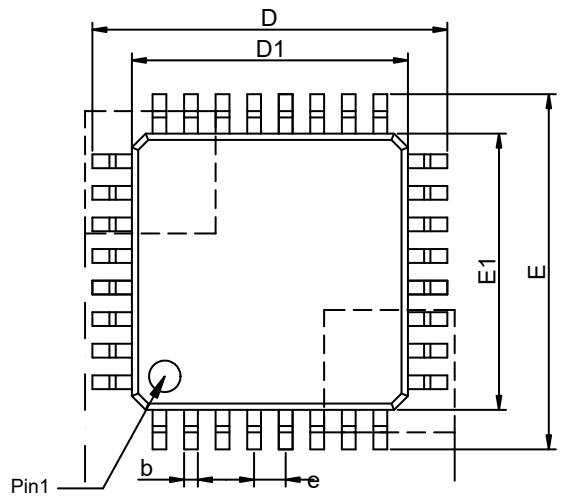
(Unit of Measure=millimeters)

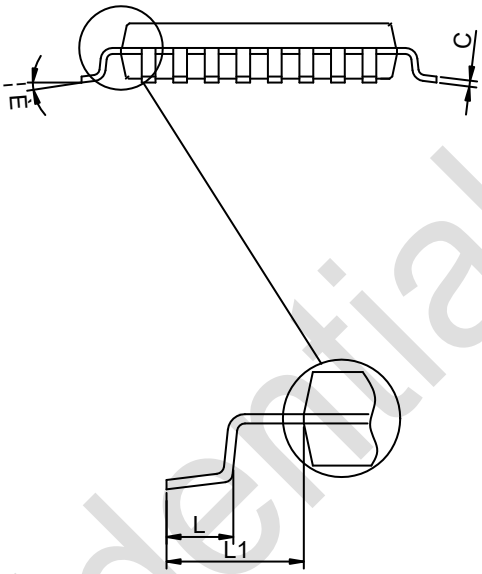
Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	-	0.020	0.050
b	0.150	0.200	0.250
c	0.200REF		
D	4.900	5.000	5.100
D2	3.600	3.700	3.800
E	4.900	5.000	5.100
E2	3.600	3.700	3.800
e	0.400BSC		
Nd	3.600BSC		
Ne	3.600BSC		
L	0.350	0.400	0.450

Note：1. Dimensions are not to scale

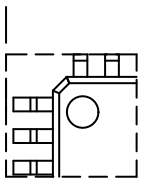
	TITLE	DRAWING NO.	REV
PUYA	Puya QFN40L 5X5X0.75-0.4PITCH POD	QRPD-0075	1.1

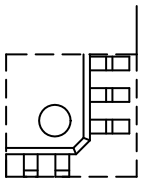
6.5. LQFP32 package size

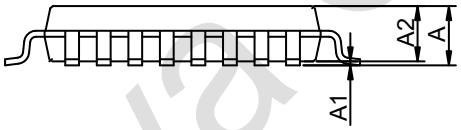




Note 2:







Common Dimensions

(Unit of Measure=millimeters)

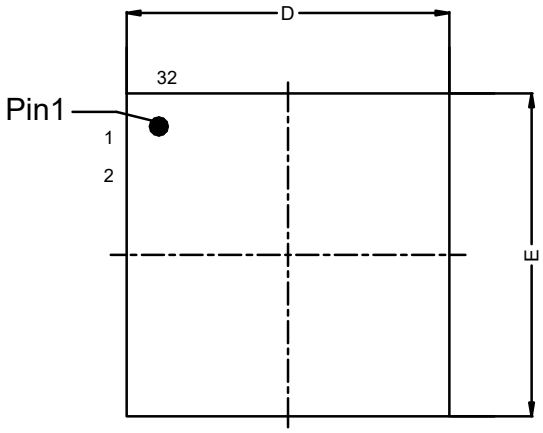
Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.300	-	0.450
c	0.100	-	0.200
D	8.800	9.000	9.200
D1	6.800	7.000	7.200
E	8.800	9.000	9.200
E1	6.800	7.000	7.200
e		0.800BSC	
L	0.450	-	0.750
L1		1.000REF	
¦È	0	-	7¡ã

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

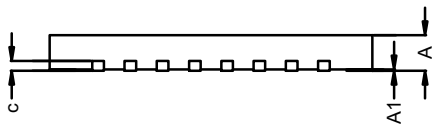
	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP32L 7x7X1.4-0.8PITCH	QRPD-0040	1.0

6.6. QFN32(5*5) package size

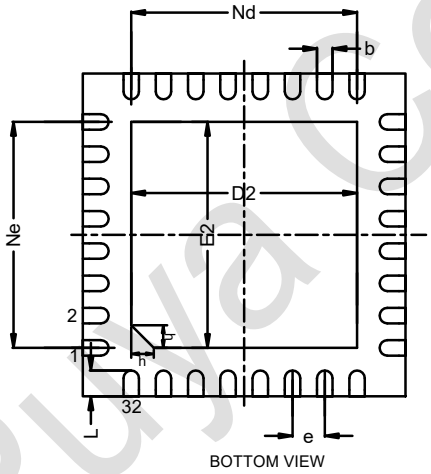
TOP VIEW



SIDE VIEW



BOTTOM VIEW



BOTTOM VIEW

Common Dimensions

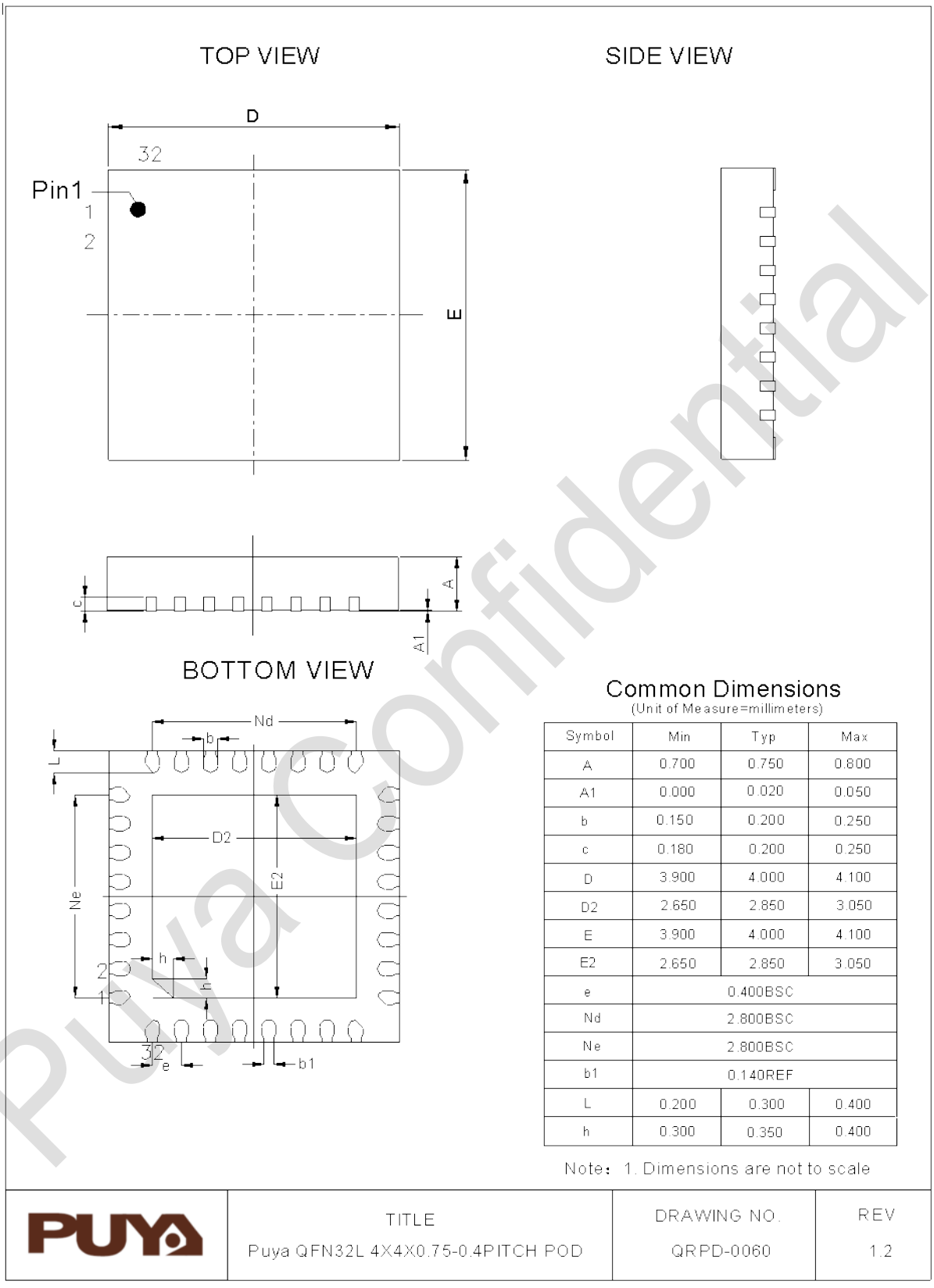
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0	0.020	0.050
b	0.180	0.250	0.300
c	0.200REF		
D	4.900	5.000	5.100
D2	3.400	3.500	3.600
E	4.900	5.000	5.100
E1	3.400	3.500	3.600
e	0.500BSC		
Nd	3.500BSC		
L	0.350	0.400	0.450
h	0.300	0.350	0.400

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN32L 5x5X0.75-0.5PITCH POD	QRPD-0042	1.0

6.7. QFN32(4*4) package size



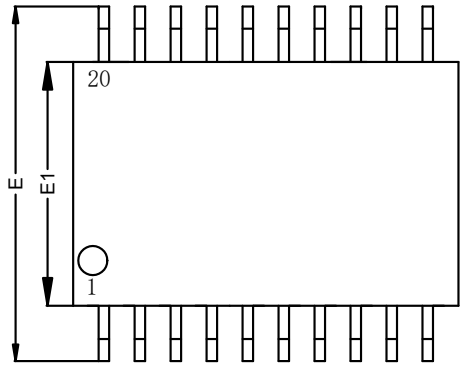
Common Dimensions
(Unit of Measure=millimeters)

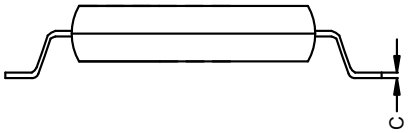
Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.650	2.850	3.050
E	3.900	4.000	4.100
E2	2.650	2.850	3.050
e	0.400BSC		
Nd	2.800BSC		
Ne	2.800BSC		
b1	0.140REF		
L	0.200	0.300	0.400
h	0.300	0.350	0.400

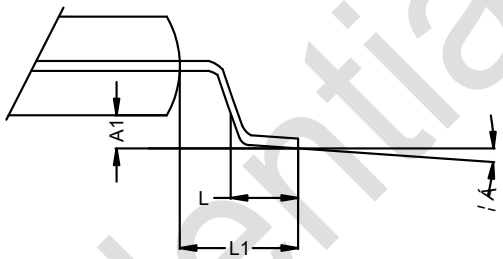
Note：1. Dimensions are not to scale

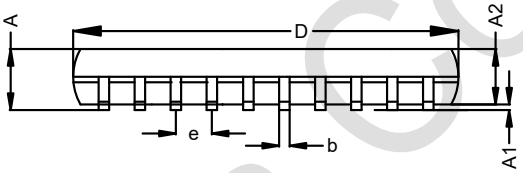
	TITLE	DRAWING NO.	REV
PUYA	Puya QFN32L 4X4X0.75-0.4PITCH POD	QRPD-0060	1.2

6.8. TSSOP20 package size









Common Dimensions

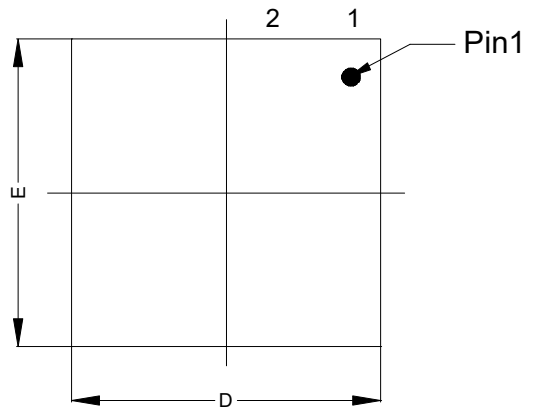
(Unit of Measure=millimeters)

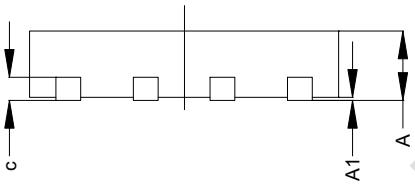
Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
b	0.200	-	0.280
c	0.090	-	0.200
D	6.400	6.500	6.600
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	0.650BSC		
L	0.450	0.600	0.750
L1	1.000REF		
¦È	0	-	8¡ã

Note：1. Dimensions are not to scale

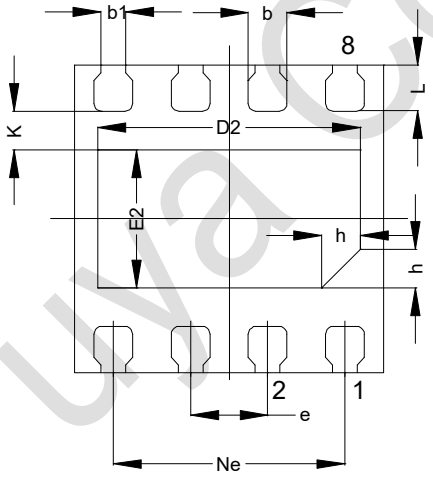
	TITLE	DRAWING NO.	REV
PUYA	Puya TSSOP20 POD	QRPD-0043	1.0

6.9. DFN8(2*2*0.45) package size





BOTTOM VIEW



Common Dimensions

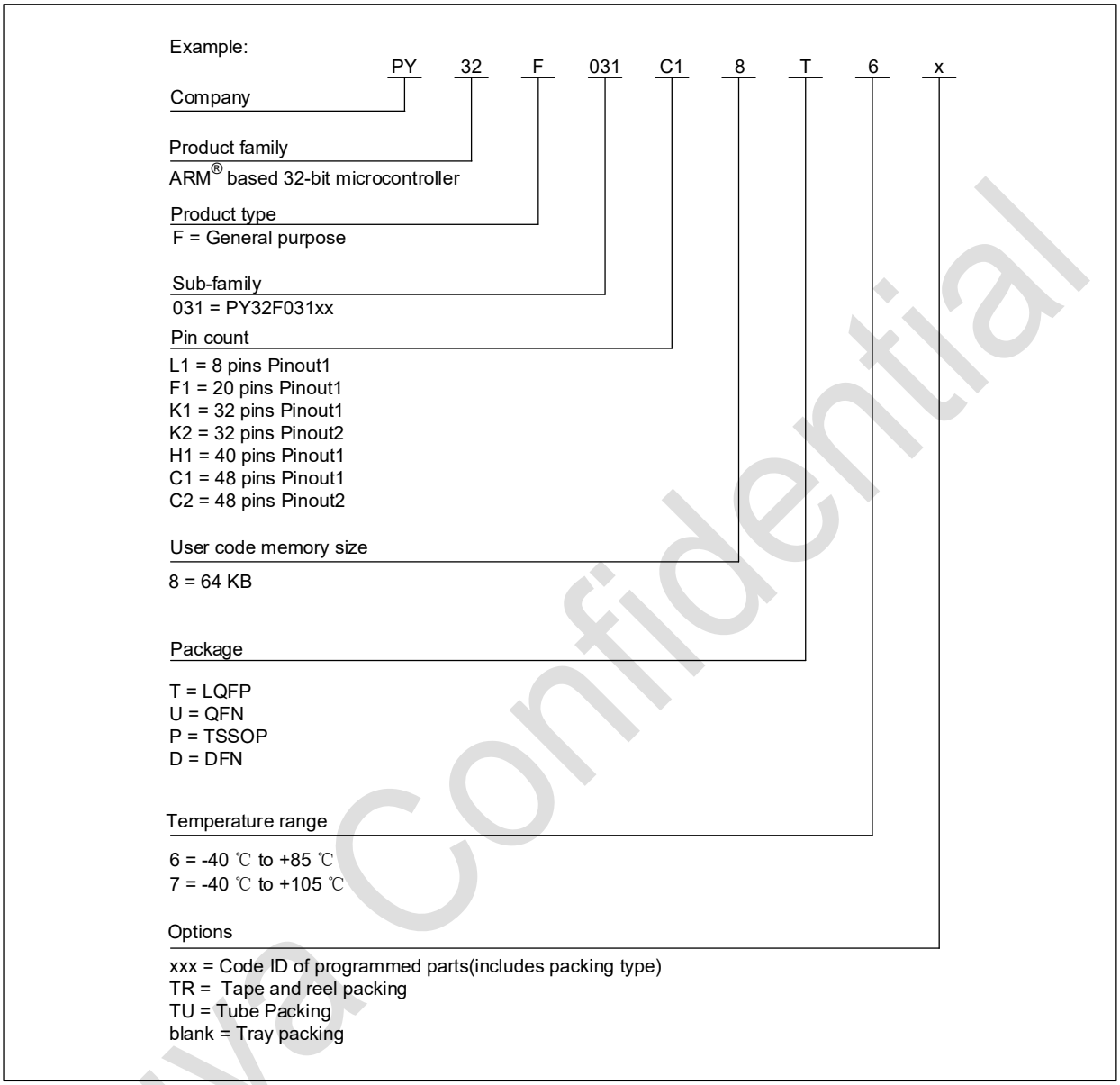
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.400	0.450	0.500
A1	0.000	0.020	0.050
b	0.200	0.250	0.300
b1	0.110	0.160	0.210
c	0.100	0.150	0.200
D	1.900	2.000	2.100
D2	1.600	1.700	1.800
e	0.500BSC		
Ne	1.500BSC		
E	1.900	2.000	2.100
E2	0.800	0.900	1.000
L	0.250	0.300	0.350
h	0.200	0.250	0.300
K	0.200	0.250	0.300

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya DFN8L 2X2X0.45-0.5PITCH POD	QRPD-0083	1.0

7. Ordering information



8. Version history

Version	Date	Descriptions
V0.18	2025.05.29	1. Initial version

Puya Semiconductor Co., Ltd.